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IMPLEMENTATION AND TESTING OF A NEW
16-PSK TRANSMITTER

by

George S. Brock

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The work reported herein deals with the design, implementation, and testing the performance of a specific 16-PSK trans-itter for use in conjunction (in future tests) with a specific direct bit detection receiver. A specific design procedure is utilized r generating sets of 2^n phase shifted sinusoids with constant phase difference, each of which represents an n bit symbol. ne design of the 16-PSK transmitter is extendable to the implementation of higher order M-PSK transmitters, i.e., M = ', 64, etc. The procedure utilizes a shift register and associated digital devices to produce a set of square waveforms each which is equally and successively delayed by a fixed time increment. Frequency selective filtering is then employed to nvert this collection of square waves to a set of sinusoids while maintaining the time and therefore the desired phase re-tionship amongst members of the set. This implementation made it possible to produce an offset 16-PSK signal nstellation whose members were all of equal amplitude and possessed the desired phase relationships to within one tenth a degree. The signal constellation was highly stable and displayed an average phase drift amongst its members of less than ree tenths of a degree after five and one half hours of operation. Photographs of signals in the time domain and displays signals in the frequency domain are presented in order to highlight the important features of the system's performance.

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Implementation and Testing of a New 16-PSK Transmitter

by

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Major, United States Marine Corps
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Submitted in partial fulfillment of the
requirements for the degree of

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December 1988

ABSTRACT

The work reported herein deals with the design, implementation, and testing the performance of a specific 16-PSK transmitter for use in conjunction (in future tests) with a specific direct bit detection receiver. A specific design procedure is utilized for generating sets of 2^n phase shifted sinusoids with constant phase difference, each of which represents an n bit symbol. The design of the 16-PSK transmitter is extendable to the implementation of higher order M-PSK transmitters, i.e., M = 32, 64, etc. The procedure utilizes a shift register and associated digital devices to produce a set of square waveforms each of which is equally and successively delayed by a fixed time increment. Frequency selective filtering is then employed to convert this collection of square waves to a set of sinusoids while maintaining the time and therefore the desired phase relationship amongst members of the set. This implementation made it possible to produce an offset 16-PSK signal constellation whose members were all of equal amplitude and possessed the desired phase relationships to within one tenth of a degree. The signal constellation was highly stable and displayed an average phase drift amongst its members of less than three tenths of a degree after five and one half hours of operation. Photographs of signals in the time domain and displays of signals in the frequency domain are presented in order to highlight the important features of the system's performance.

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I. INTRODUCTION

A. PROBLEM STATEMENT

This thesis addresses the design and implementation of a transmitter to generate 16-PSK modulated signals. The transmitter implementation is geared toward compatibility with a specific receiver design; however, the signals generated by the implemented system are of sufficient generality to be usable in most applications involving receivers for phase shifted sinusoids. The transmitter must be capable of shifting the phase of a reference sinusoid by 16 equally spaced angle increments, while also providing two additional sinusoidal functions to be used in testing the performance of a coherent receiver. It is desirable that the design be capable of extensions to higher order implementations; therefore, the transmitter implementation is a proof of concept effort that could be applied to the design of PSK modulated signals of M-ary type, where $M = 2^n$ and $n = 5, 6, \ldots$.

B. BACKGROUND

The work was begun with a final objective of testing the performance of a specific receiver design for 16-PSK modulated signals. An intermediate objective in this effort is the implementation of a transmitter capable of producing the signals necessary for testing the performance of this specific receiver. Previous work has dealt with the generation of lower order PSK signals [Refs. 1: pp. 22-23, 2: pp. 13-17]. The applicability of these previous transmitter designs to a 16-PSK system appeared either lacking in phase generation accuracy, or cumbersome in physical implementation. The search for a more accurate and efficient transmitter brought about the design outlined in this thesis. The premise of the design was that digital techniques could be employed to generate an ensemble of analog waveforms possessing the desired phase relationships that could be maintained accurately while operating at waveform switching rates of several thousand per second. The design appeared to possess the accuracy and efficiency required for this and higher order systems; therefore, the implementation was undertaken to prove the concept and also uncover any constraints that could occur in the process of transferring a paper design into hardware.[Ref. 3: pp. 1-3]

C. CONTENTS

The format for the presentation of this thesis begins with a short presentation on the theoretical foundations associated with 16-PSK modulated signals. Chapter III focuses on the transmitter design, and the details of the hardware implementation are explained along with an alternate implementation focused on a more accurate scheme for phase rotating the sinusoidal waveforms required by the (as yet not implemented) coherent receiver. System performance is then analyzed with respect to signal accuracy and stability. Photographs of waveforms and spectra generated by this implementation are presented in Chapter IV in order to highlight the performance of the hardware. The final chapter is devoted to summarizing the work carried out and highlighting its application to various digital communication system implementations. An appendix is included in order to provide information relating to the theoretical operation and performance of the receiver with which the transmitter is designed to operate.

II. THEORETICAL FOUNDATIONS

A. PHASE SHIFT KEYING

Phase shift keying (PSK) is a bandwidth efficient method of modulating a carrier signal with digital data. The modulation process consists of shifting the phase of a reference carrier to represent a unique data state. Binary PSK (BPSK) is the most straightforward and best known phase modulation scheme. One bit of data is used to represent two possible data states. The phase of the carrier is shifted by zero or 180 degrees in order to represent these data states. M-PSK is a method of modulating a carrier with a unique symbol. Each symbol consists of two or more bits. The number of unique data states is defined as $M = 2^n$, where n represents the number of bits which comprise the symbol. A 16-PSK scheme would utilize a symbol containing four data bits to shift the phase of a carrier by 16 distinct amounts. Figure 1 shows an example of a 16-PSK signal constellation in which each sinusoidal waveform is represented as a phasor.

The bandwidth of a PSK signal depends upon the rate at which the data states (or symbols) are generated. In BPSK modulation, each bit represents a data state. If the bit rate is increased, the time duration of each bit is decreased. This compression of the data stream in time spreads the bandwidth of the signal in the frequency domain. For a given bit rate, the combination of M bits into a single symbol will increase the symbol duration to M times the bit rate duration. The spreading of the multi-level data stream in time reduces the bandwidth of the signal. PSK modulation is utilized in bandwidth limited systems in order to increase data rates and or more efficiently utilize the available system bandwidth.

B. TRANSMITTER SIGNAL CONSTELLATION

The phase relationships among sinusoids which comprise a specific transmitter signal constellation and the method by which a unique symbol is associated with a selected signal is determined by the structure of the receiver with which the transmitter is designed to operate. Figure 2 shows an off-set 16-PSK signal constellation which consists of 16 phase shifted carriers, each of which is associated with a unique four bit data symbol. The signal constellation shown in Figure 2 also displays two basis signals which are labeled cosine and sine. These basis signals are utilized by coherent PSK receivers during the demodulation process. The design and implementation described within this

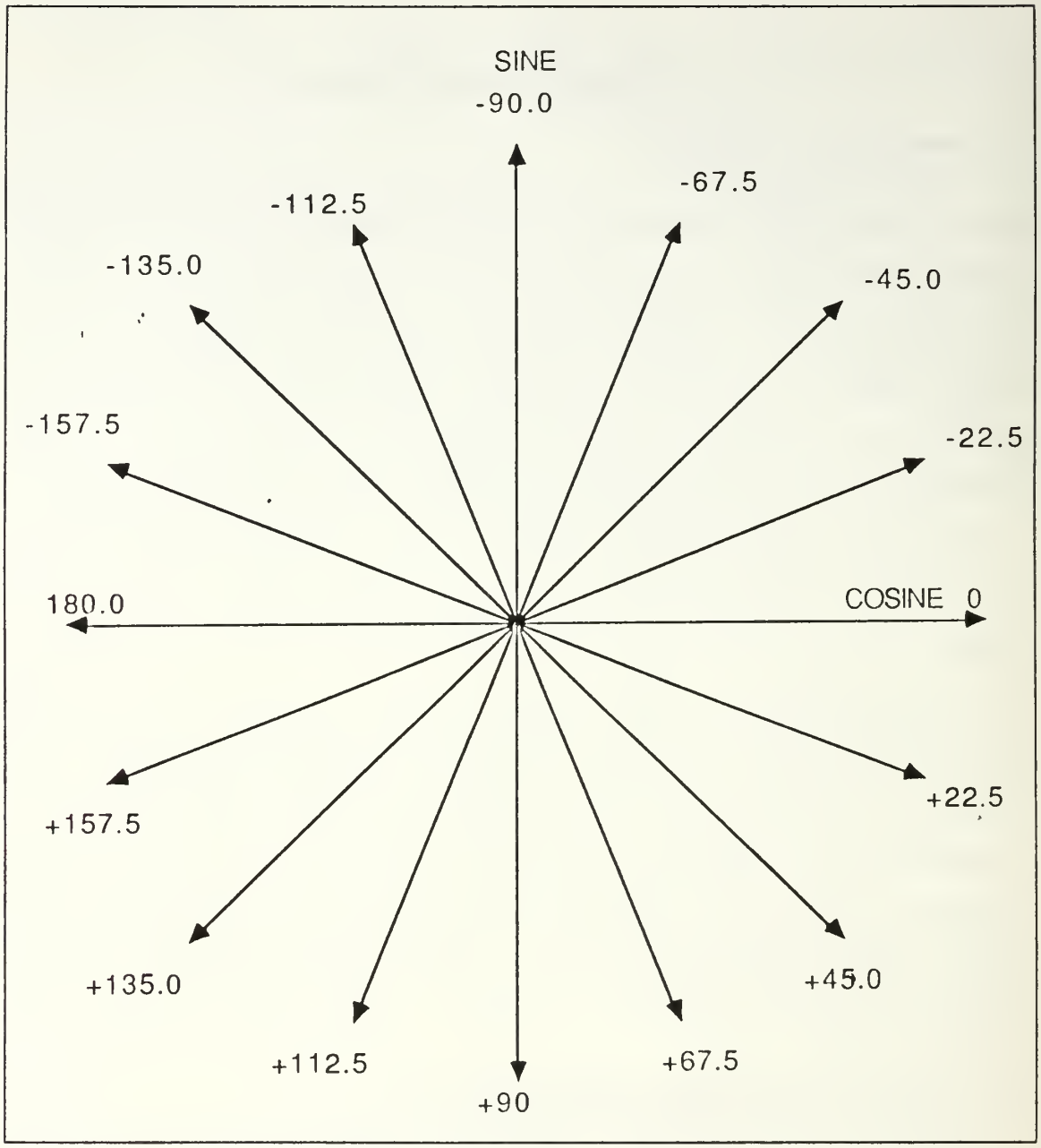

Figure 1. 16-PSK Signal Constellation

thesis is oriented toward producing a transmitter which will generate the signal/symbol constellation shown in Figure 2. The Appendix provides information relating to the theoretical operation and performance of the (not as yet implemented) coherent receiver with which the transmitter is designed to operate.

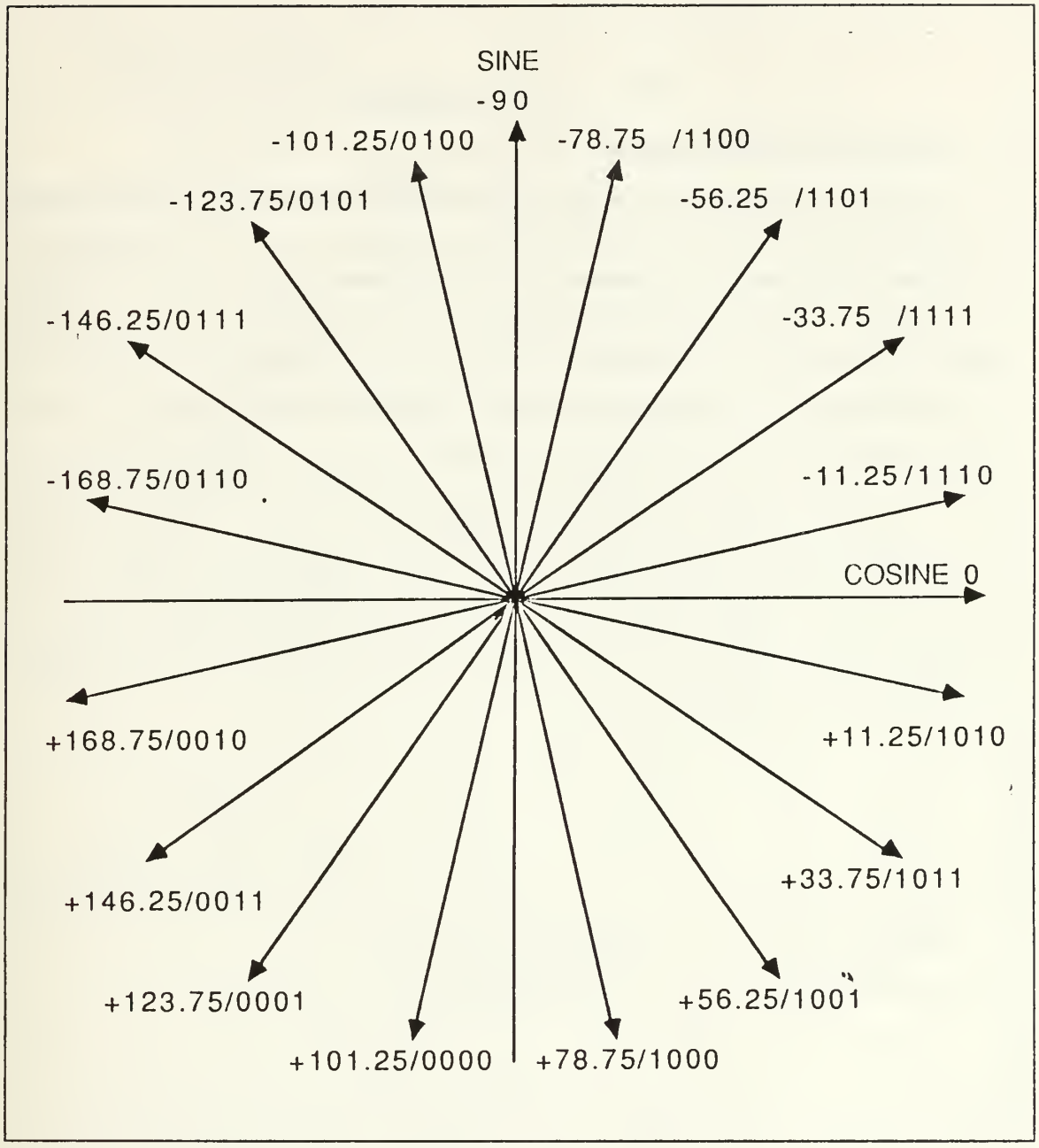

Figure 2. Off-Set 16-PSK Signal Constellation

III. SYSTEM DESIGN

A. SYSTEM BLOCK DIAGRAM

The design of the physical system involved the implementation of the block diagram elements shown in Figure 3. The first step in the design process was oriented toward generating signals having the structure shown in the constellation diagram of Figure 1. The generation of this group of signals began with the utilization of digital techniques to form a collection of unipolar square waves, each appropriately delayed in time by the use of a shift register. Filtering these square waveforms would then yield the desired signal constellation as explained in the sequel [Ref. 3: p. 1]. The basis functions are generated via the previously described technique in which an additional phase rotation by an appropriate phase increment is implemented in order to produce the signal constellation of Figure 2. Each signal vector within the constellation of Figure 2 is then associated with a specific four bit data symbol by the multiplexer. That is, the multiplexer output consists of one of the desired 16-PSK signals for each unique grouping of four bits of the data.

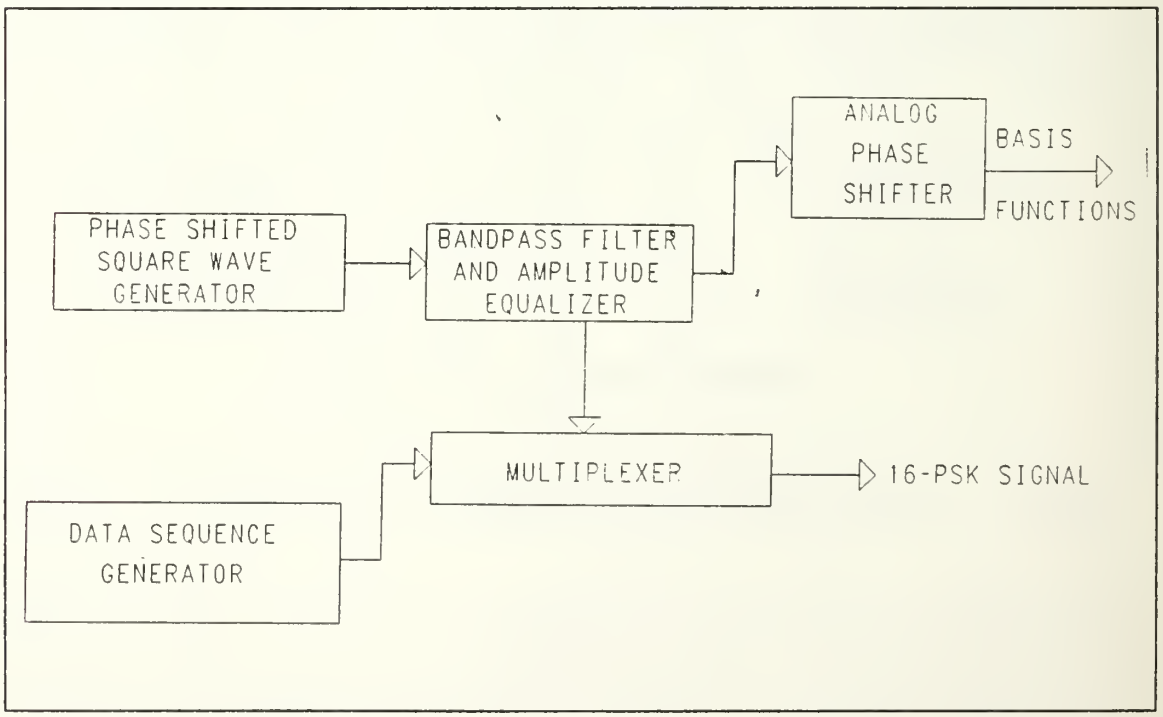

Figure 3. 16-PSK Transmitter Block Diagram

1. Signal Constellation

a. Phase Shifted Square Waves

The procedure used to generate the set of 16 phase shifted square waves is based on the conceptual design outlined in Reference 3. The system block diagram for the implementation of this design is shown in Figure 4, and a timing diagram of the signals at different points within the system is presented in Figure 5. The letters designating the waveforms in Figure 5 relate their measurement location to the block diagram in Figure 4. The amplitude of each waveform transitions between levels of zero and five volts. The shift register and counters of Figure 4 are rising edge triggered, while the flip flops are falling edge triggered. Referring to Figure 5, the diagram shows the one microsecond delay that exists between waveforms A and B, as well as between waveforms B and H, as a result of clocking the input waveform through successive stages of the shift register. The waveforms B and H are then divided in frequency by the counter/AND gate combinations, to produce the waveforms K and E as shown in the timing diagram. Tracing the output of the first stage of the shift register, as shown in Figures 4 and 5, reveals that the counter output increments with the arrival of the rising edge of waveform B, and counts to three in binary before resetting to zero and starting over the counting process. The diagram of waveforms C and D demonstrates this process. As the count of three is reached, the output of the AND gate becomes high and remains high until the the next leading edge of waveform B arrives. The AND gate output is then used as a clock pulse for the Toggle (T) flip flop. The output of the T flip flop changes states with the falling edge of each clock pulse. The final set of successively delayed square waves correspond to the Q and $\overline{Q}$ outputs of the flip flops. These waveforms are designated V1 and $\overline{V1}$ through V8 and $\overline{V8}$ in Table 1. The stage to stage delay between waveforms B and H is preserved during the process of frequency division, and can be observed by comparing waveforms E and K in Figure 5. This delay is then transferred through the flip flops to the square waves. The final set of waveforms which appear at the output of the flip flops share a common fundamental frequency of 62.5 kHz. This characteristic frequency is the operating carrier frequency of the transmitter and is defined as f_0. The characteristic period of the final set of waveforms is the inverse of their frequency and is defined as $T_0 = 1/f_0$. Table 1 displays the time delays of the final set of square waves, the shift register stage from which the waveforms originated,

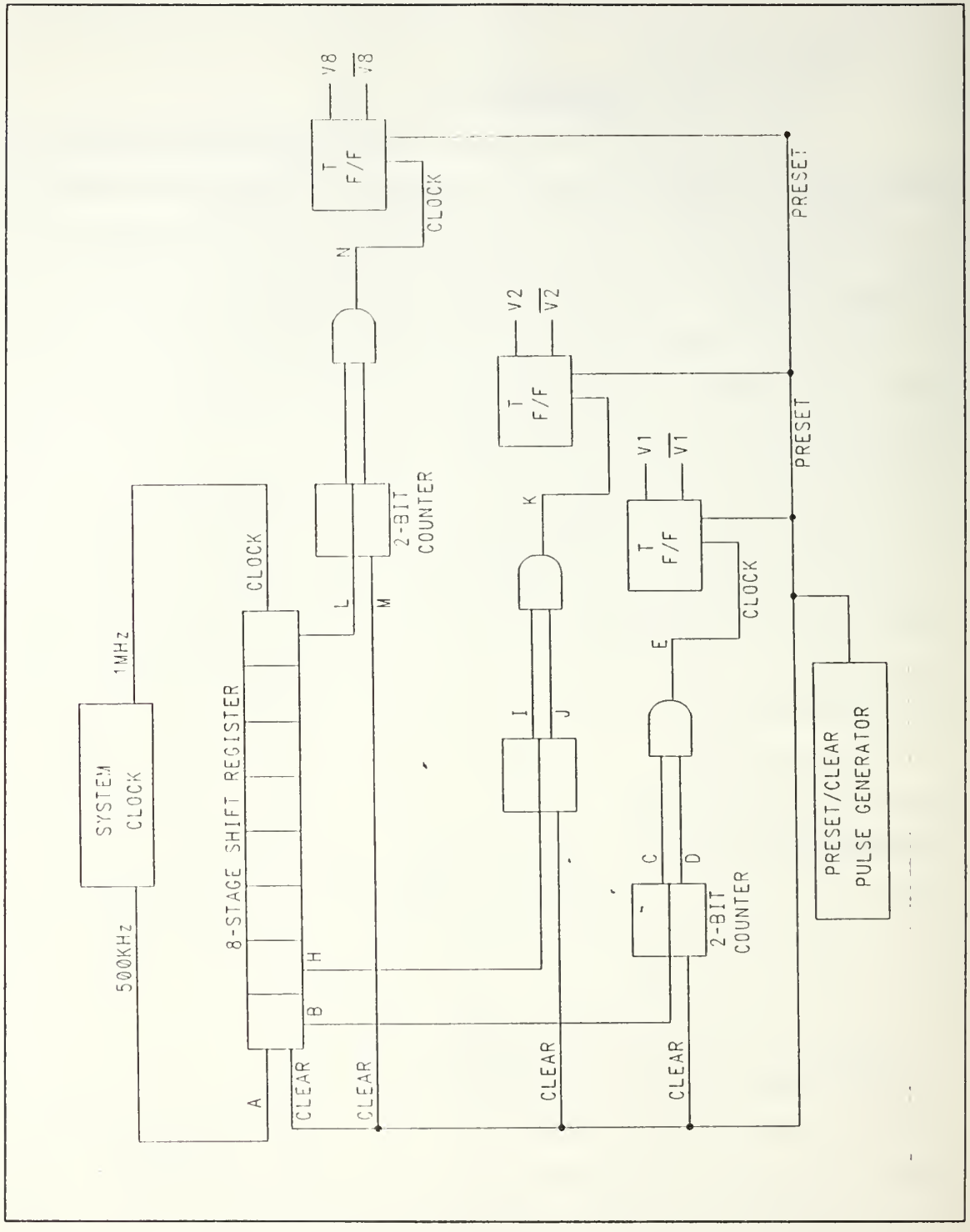

Figure 4. System to Generate a Set of Phase Shifted Square Waves

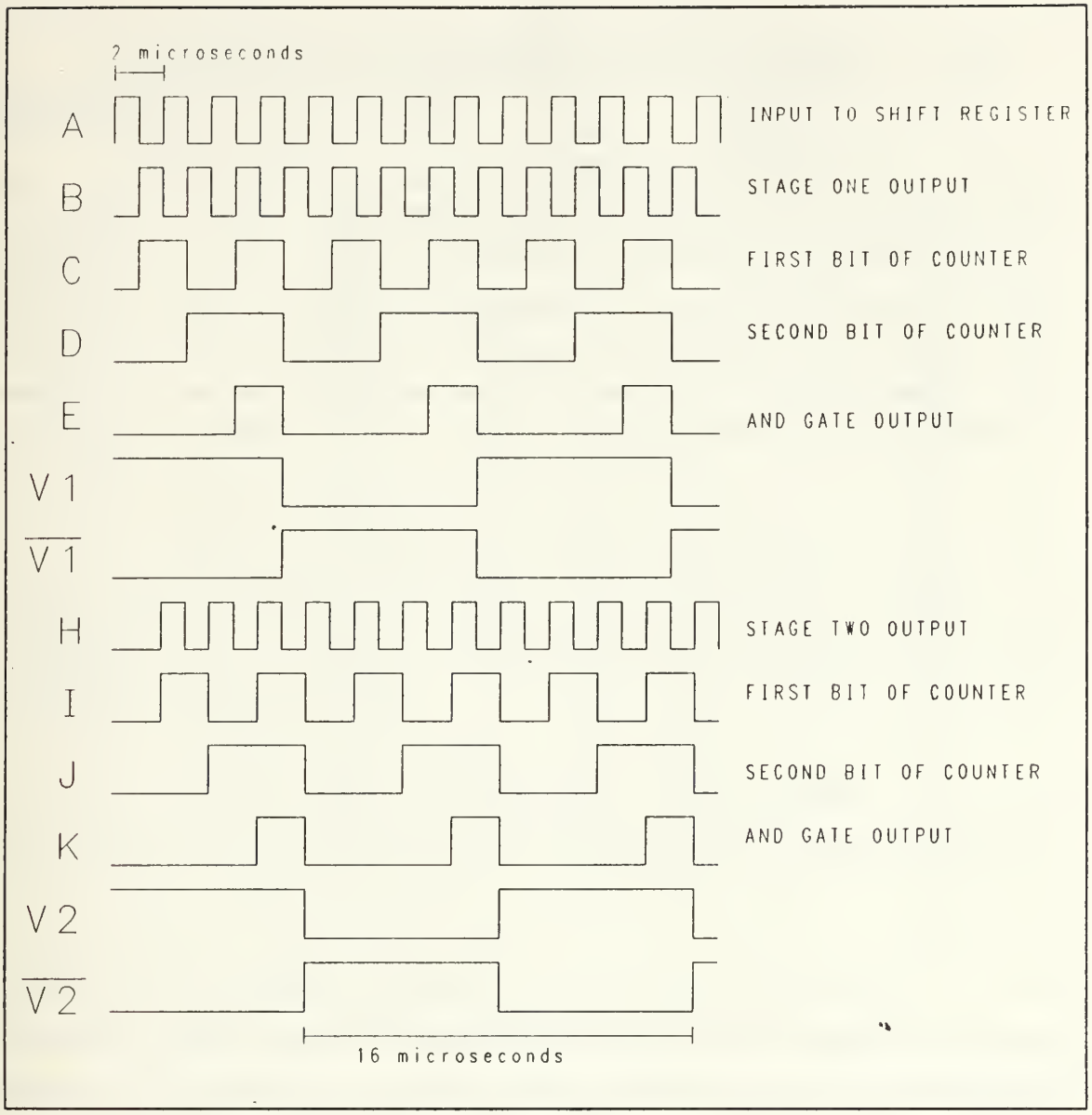

Figure 5. Square Wave Generation Timing Diagram

and associates each time delayed square wave with its post filtered phase shifted sinusoidal counterpart.

Table 1. SQUARE WAVE STAGE/TIME/PHASE RELATIONSHIPS

Waveform	Shift Register Stage Origin	Delay (microseconds)	Phase Shift of Corresponding Sinusoid (degrees relative to cosine and rotated cosine respectively)	
V1	1	1	-22.5	-33.75
V2	2	2	-45	-56.25
V3	3	3	-67.5	-78.75
V4	4	4	-90	-101.25
V5	5	5	-112.5	-123.75
V6	6	6	-135	-146.25
V7	7	7	-157.5	-168.75
V8	8	8	180	+168.75
$\overline{V1}$	1	9	+157.5	+146.25
$\overline{V2}$	2	10	+135	+123.75
$\overline{V3}$	3	11	+112.5	+101.25
$\overline{V4}$	4	12	+90	+78.75
$\overline{V5}$	5	13	+67.5	+56.25
$\overline{V6}$	6	14	+45	+33.75
$\overline{V7}$	7	15	+22.5	+11.25
$\overline{V8}$	8	16	0	-11.25

This design procedure may be modified and extended to produce incrementally phase delayed square waves which may be filtered to generate PSK signal constellations with each signal representing k binary bits. In general, a set of 2^k phase shifted waveforms may be generated with a $2^{(k-1)}$ stage shift register. The output of each individual shift register stage is then divided down in frequency by a $(k - 2)$ bit counter whose output is then processed by a $(k - 2)$ input AND gate. If the period T of the shift register input waveform is such that $T^{-1} = 2^{(k-1)} f_o$, then the resultant square wave array after frequency division will have a fundamental frequency of f_o , and each square waveform will be delayed with respect to every other such waveform by an integer multiple of $T_o / 2^k$ seconds [Ref. 3: p. 2]. This generalized procedure was employed in order to implement the system outlined in Figure 4 for the parameter $k = 4$; $2^k = 16$, $2^{(k-1)} = 8$, and $(k - 2) = 2$. The choice of operating carrier frequency determined the

frequency of the square wave input to the first stage of the shift register as 500 kHz = $8f_o$. The period of the final array of square waves is $1/f_o = T_o = 16$ microseconds, while the delay amongst the resulting waveforms is an integer multiple of $T_o/16 = 1$ microsecond.

A critical element of the circuit of Figure 4 is the preset/clear pulse generator. The pulse clears the shift register (sets the contents of each stage to zero) and initializes the time delay between the input and successive stages. The pulse also clears the two-bit counters, and presets the state of all eight T flip flops. This presetting ensures that Vn is high and $\overline{\text{Vn}}$ is low when the input is clocked into the first stage of the shift register. If the phase relationship among the waveforms is lost during experimentation, activating the pulse generator will regenerate the desired waveform ensemble.[Ref. 3: p. 3]

b. Phase Shifted Sinusoids

The process of converting the collection of delayed square waves into a set of phase shifted sinusoids is accomplished through frequency selective filtering. This approach is based on the fact that a periodic square wave of period $T_o = 1/f_o$ may be represented by the Fourier series

$$v(t) = \frac{4}{\pi}\cos 2\pi f_0 t + \frac{4}{3\pi}\cos(3)2\pi f_0 t + \frac{4}{5\pi}\cos(5)2\pi f_0 t + \ldots. \qquad (3.1)$$

This series possesses components at the fundamental frequency and at odd multiples of this frequency. The specific waveforms generated by the system of Figure 4 are DC offset square waves which oscillate between zero and five volts. The Fourier series representing these waveforms will possess an additional DC component which is blocked in the process of recovering the fundamental frequency of these waveforms via bandpass filtering. The circuit diagram of the specific bandpass filter chosen to perform this task is shown in Figure 6.

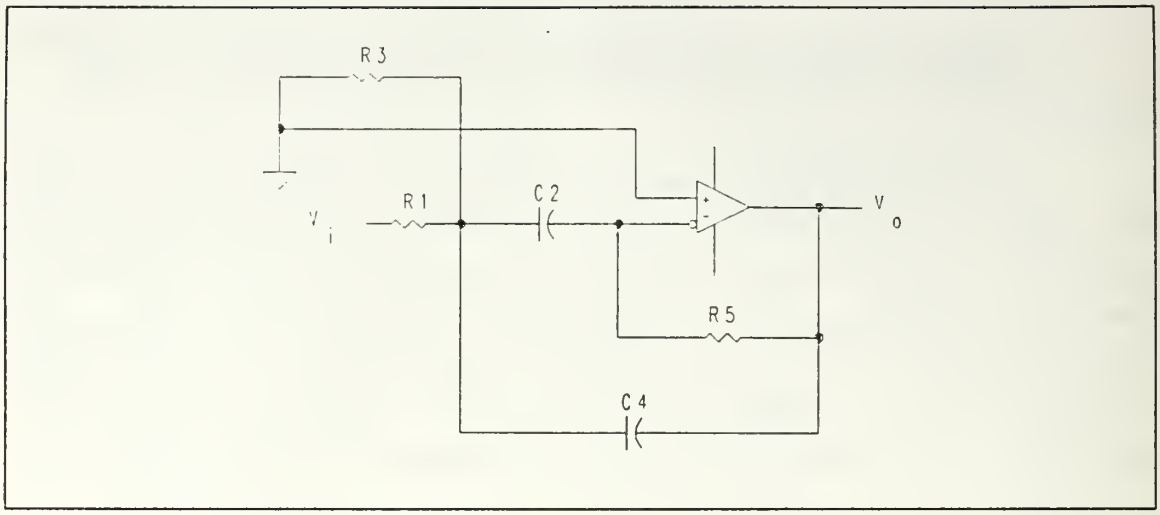

Figure 6. Active Bandpass Filter

The selection of component values in this design define the filter characteristics of center frequency (f_c), gain (G), and the parameter Q, which is a measure of the rate at which the filter rolls off and is defined as

$$Q = \frac{f_c}{3dB\ bandwidth} \tag{3.2}$$

In order to attain the desired attenuation, a Q value of five was selected [Ref. 4: p. 145]. A design gain of 1.0 was used for convenience. The process of selecting component values was initiated by setting C1 = C2 = .001 microFarad, and substituting into the following set of equations in order to specify all the component values of the filter.[Ref. 4: pp. 140-142]

$$G = \frac{R5}{2R1} \tag{3.3}$$

$$2\pi f_c = \sqrt{\frac{1}{R5C^2}\left(\frac{1}{R1} + \frac{1}{R5}\right)} \tag{3.4}$$

$$R1 = \frac{Q}{GC\,2\pi f_c} \tag{3.5}$$

$$R3 = \frac{Q}{(2Q^2 - G)C\,2\pi f_c} \tag{3.6}$$

$$R5 = \frac{G}{QC\,2\pi f_c} \tag{3.7}$$

The procedure yields the values listed in Table 2. The computed values were then used to select available standard resistor values for the implementation of the filter. The input to each such bandpass filter consists of one member of the collection of phase delayed equal amplitude waveforms. It is critical that the phase and amplitude relationships amongst these signals be preserved in the filtering process. Maintaining these parameter relationships precisely would require implementation of 16 identical filters. The possibility of producing identical filters with standard lumped components is highly unlikely due to variations in these components. Thus the filtering process must possess sufficient flexibility to overcome variations in individual filter characteristics. In general, the phase and amplitude characteristics of bandpass filters are closely related to the filters' center frequency, with the amplitude response peaking at the center frequency and then rolling off as frequency increases above and decreases below the center frequency. The filter phase characteristics can be made to correspond to a zero phase shift at the center frequency (180 degrees if an inverting configuration is used) while the phase shift behaves as a linear function of frequency across the filter passband. All input square waveforms have a fundamental frequency of 62.5 kHz, while each filter is designed to match its own center frequency f_c to this fundamental frequency f_o. However, variations in stock component values and in each operational amplifier's characteristics, will yield center frequency variations in the filters. The center frequency of each filter must be adjusted to match the fundamental frequency of the input waveforms in order to maintain appropriate phase relationships throughout the filtering process. The process of matching the center frequency of each filter to the fundamental frequency of the set of square waves is accomplished by observing that the dominant resistive element in Equation 3.4 is R5. Varying R5 will allow adjustments in the center frequency and the phase characteristics of the filter. Equation 3.3 indicates that a change in values assigned to R5 will also change the filter gain and therefore the amplitude of the output sinusoid. This resulting amplitude variation is removed by cascading a variable gain operational amplifier with the bandpass filter of Figure 6.

Table 2. COMPUTED AND STANDARD RESISTOR VALUES

Resistor	Computed Value (kΩ)	Standard Value (kΩ)
R1	12.36	12
R3	0.252	0.240
R5	24.72	24

c. Basis Functions

The procedure outlined in the previous section was used for the implementation of a system for the generation of the signal constellation shown in Figure 1. The signals represented by the constellation of Figure 2 can now be generated by reproducing the cosine and sine signals which are represented by phasors in Figure 1, and phase rotating these reproduced signals clockwise by 11.25 degrees. These two new signals become the basis functions of cosine and sine shown in Figure 2 which will be utilized by the (as yet not implemented) coherent receiver. The regeneration of the unshifted cosine and sine signals of Figure 1 is accomplished by employing the procedure described in the previous section. These replica cosine and sine signals are then applied to the analog phase shifter shown in Figure 7 in order to produce the required +11.25 degree phase shift [Ref. 2: pp. 13-16].

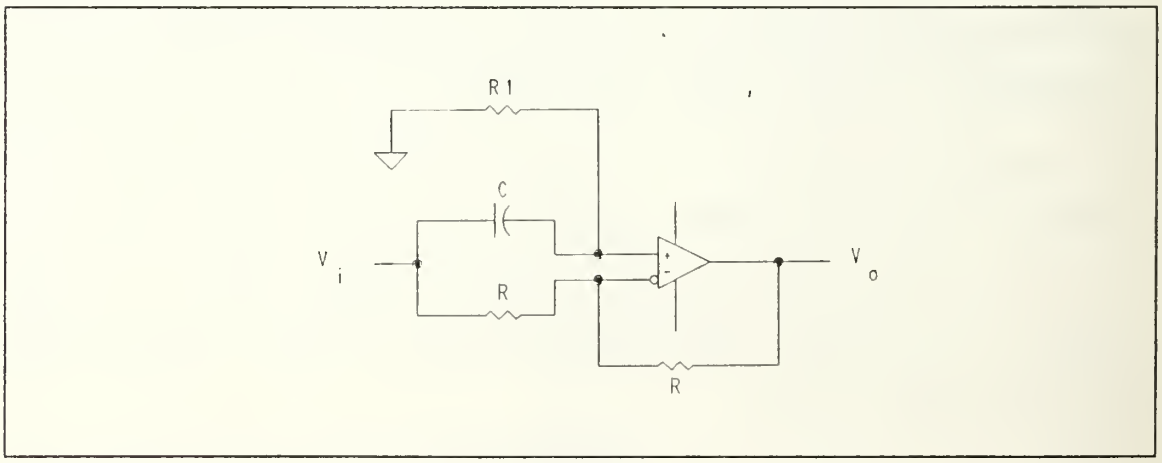

Figure 7. Analog Phase Shifter

The voltage transfer function of the phase shifter is

$$\frac{v_o}{v_i} = \frac{R1 + j\left(\frac{1}{2\pi f_c}\right)}{R1 - j\left(\frac{1}{2\pi f_c}\right)} \tag{3.8}$$

so that

$$\left| \frac{v_o}{v_i} \right| = 1 \tag{3.9}$$

and

$$\angle\phi(2\pi f_c) = 2\tan^{-1}\left(\frac{C}{R1\ 2\pi f_c}\right) \tag{3.10}$$

In order to obtain the desired circuit phase response, a capacitance value of .001 microFarad is employed in conjunction with an R1 value of 25.85 kohms. The design alteration required to produce the basis functions consisted of adding a third stage to the two stage bandpass filter and amplitude attenuator which is utilized to generate the signals represented by Figure 1.

2. Data Sequence

The transmitter design requires four data bits to select for transmission one of the 16 sinusoids shown as phasors in Figure 2. To fully test the implementation, it is desirable that this data stream be random in nature and range over symbol states between 0000 and 1111. The eight stage feedback shift register (FSR) of Figure 8 was selected to perform this task. An FSR, when appropriately configured, will generate a stream of bits known as an M-sequence, consisting of a periodic pseudorandom stream of binary bits with period L bits long. For such an M-sequence, $L = 2^n - 1$, where n represents the number of shift register stages. The all zero state is a prohibited FSR state, causing L to not equal 2^n. Should the FSR inadvertently fall into the all zero state, it would permanently remain in that state unless detecting and resetting circuitry is incorporated in the design. The configuration shown in Figure 8 will produce an M-sequence of length 255 [Ref. 5: p. 280] with four data bits selected as one of the multiplexer inputs to be taken from stages five, six, seven, and eight of the FSR [Ref. 1: p. 68]. The implementation contains an all zero state detector which will ensure that the FSR does not permanently remain in the all zero state.

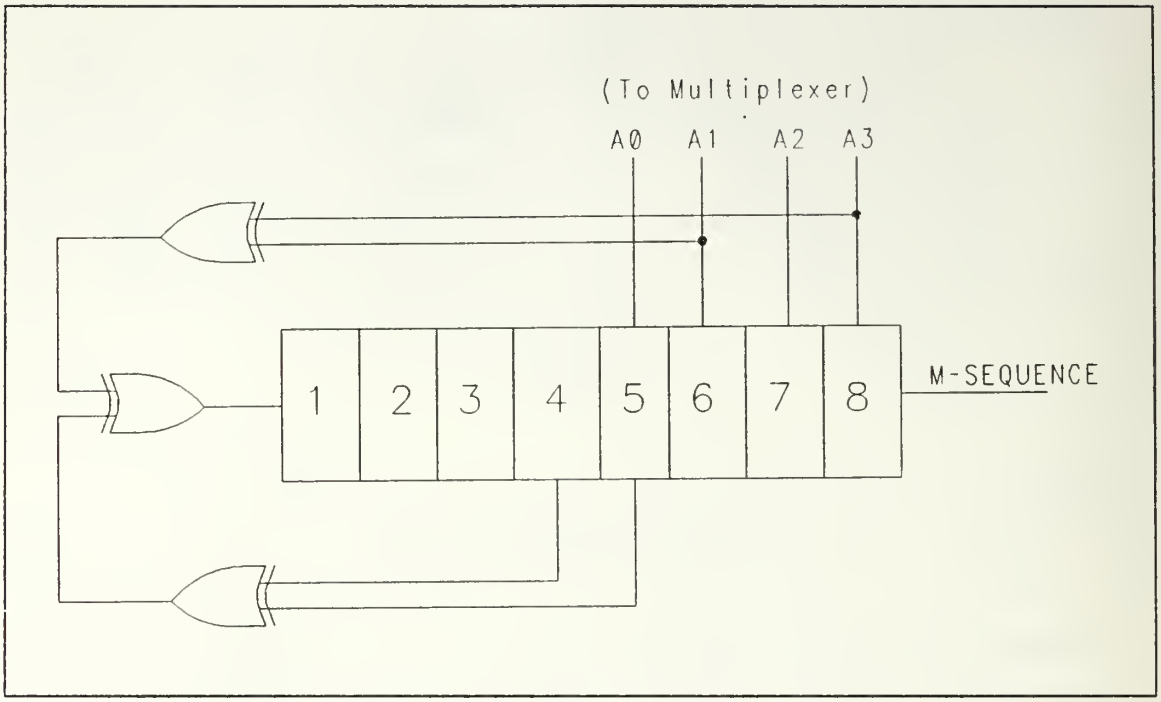

Figure 8. Block Diagram of (4,5,6,8) Feedback Shift Register

3. Multiplexer

The multiplexer is a digitally controlled analog switch that associates an n bit digital control symbol with a specific member of a set of 2^n analog signals. In this design, the analog inputs are the 16 phase shifted sinusoidal signals which which are shown in Figure 2. Four parallel digital control inputs select one of the 16 analog inputs to the multiplexer as its output. The truth table for the multiplexer is displayed in Table 3. The output of the multiplexer will be a sinusoid of constant frequency whose phase changes at the clock rate of the M-sequence generating FSR. The theoretical power spectral density of this 16-PSK signal at the multiplexer output is displayed in Figure 9.

Table 3. TRUTH TABLE WITH SYMBOL ASSIGNMENTS

Symbol				On Switch	Signal Phase (degrees)
A3	A2	A1	A0		
0	0	0	0	1	+ 101.25
0	0	0	1	2	+ 123.75
0	0	1	0	3	+ 168.75
0	0	1	1	4	+ 146.25
0	1	0	0	5	-101.25
0	1	0	1	6	-123.75
0	1	1	0	7	-168.75
0	1	1	1	8	-146.25
1	0	0	0	9	+ 78.75
1	0	0	1	10	+ 56.25
1	0	1	0	11	+ 11.25
1	0	1	1	12	+ 33.75
1	1	0	0	13	-78.75
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1	1	1	0	15	-11.25
1	1	1	1	16	-33.75

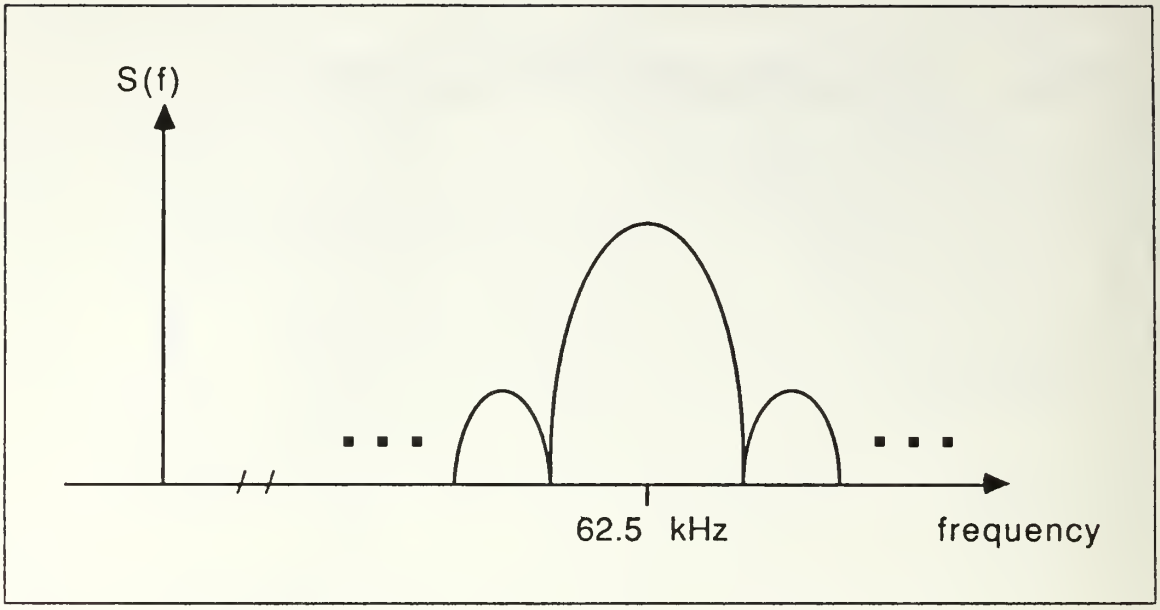

Figure 9. Power Spectral Density of 16-PSK Signal

B. IMPLEMENTATION

This section outlines the implementation of the block diagram design discussed in the previous section. Experimental techniques are highlighted, pin out diagrams are presented, and component values are specified. Throughout the implementation and testing, a Hewlett-Packard (HP) 3575A Gain/Phase meter was the main equipment item employed to obtain experimental results. The HP3575A displays the phase relationship between two signals applied at its inputs to within one tenth of a degree and their gain ratio to within one tenth of a decibel.

1. Signal Constellation

a. Phase Shifted Square Waves

The implementation of the design outlined in Figure 4 is shown in terms of pin-out diagrams in Figures 10, 11, and 12, where the system clock, preset/clear pulse generator, and the generator of the ensemble of square waves are shown, respectively. The system clock consists of the following devices:

TD309 16 MHZ Oscillator (1)

74161 Four Bit Counters (2)

The counters divide the clock frequency and also square up the clock pulses. This circuit provides a 500 kHz unipolar square wave as an input to the shift register and a 1 MHz clock signal which transfers the input through the shift register.

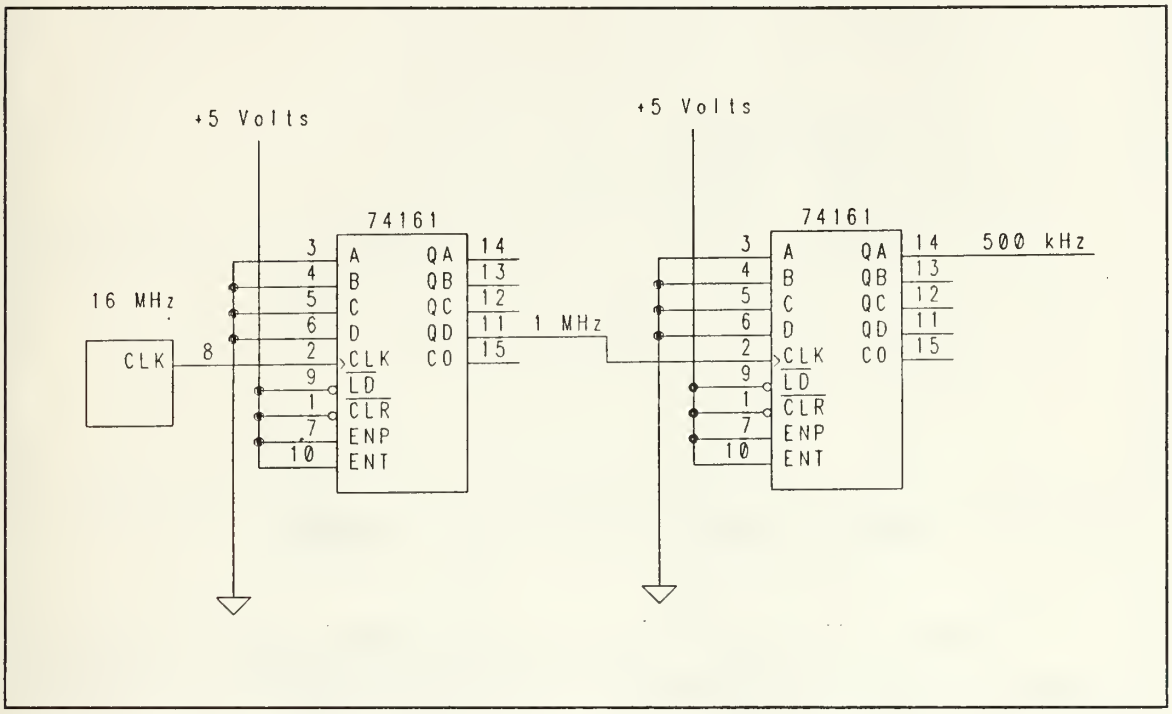

Figure 10. Implementation of System Clock

The preset/clear pulse generator consists of a 555 timer and a 7486 Quad Dual Input XOR chip. The timer is configured to generate a pulse of duration $\tau = 1.1(RC)$. In this specific implementation τ is equal to 1.1 seconds. Pin number two of the timer is connected to a five volt source through a switch. Opening the switch "fires" the one shot, and drives the output of pin number three high for 1.1 seconds. The one shot acts as a debounce for the switch and provides the sharp transition required to synchronize the system [Ref. 3: p. 3].

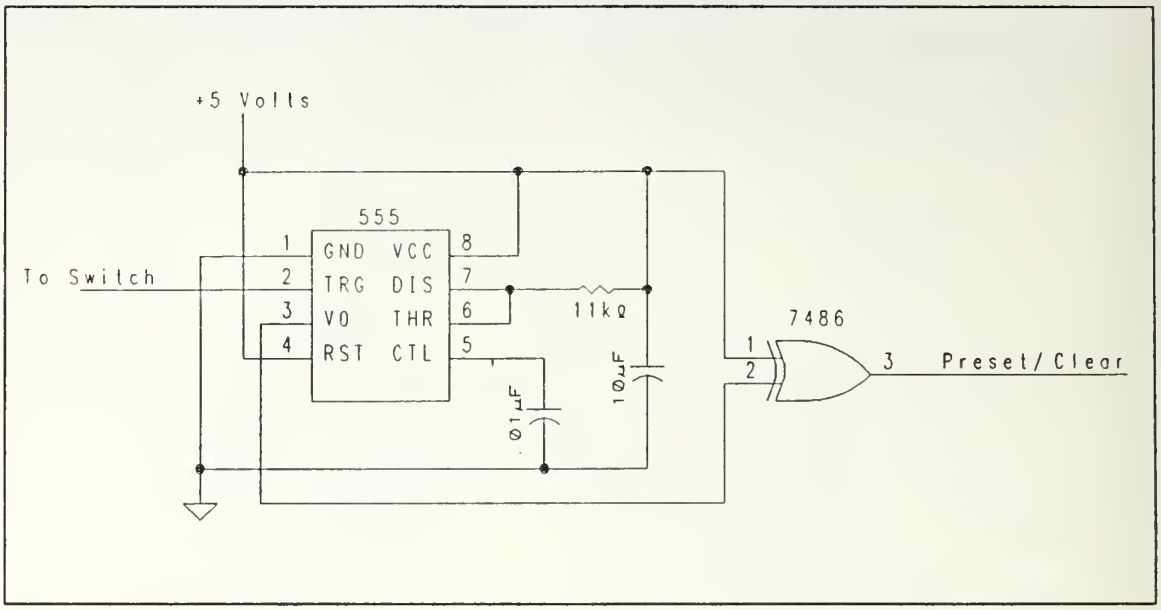

Figure 11. Implementation of Preset/Clear Pulse Generator

Figure 12 shows the implementation of the system which generates waveforms V1, V2, and their complements. The circuit shown in Figure 12 transforms the output of two stages of the shift register into four members of the final collection of square waves. The outputs of the six remaining shift register stages were processed by identical circuitry to produce the entire waveform collection. As shown in Figure 12, the generation of the square waves requires the use of the following devices:

74164 8 Stage Shift Register (1)

74161 Four Bit Counters (2)

7409 Quad Dual Input AND (1)

7476 Dual J-K Flip Flop with Preset and Clear (1)

The output of each stage of the shift register is fed into the counter. The first two bits of the counter become the input to an AND gate, so that the output of this AND gate clocks the J-K F/F. The flip flop is configured to toggle with each clock pulse. This configuration is realized by tying the J and K inputs of the flip flop to a high state.

b. Phase Shifted Sinusoids

The two stage filter implemented to convert the square wave ensemble to an array of sinusoidal waveforms is shown in Figure 13. The first stage is a bandpass filter, and the second stage provides signal amplitude adjustment. The implementation

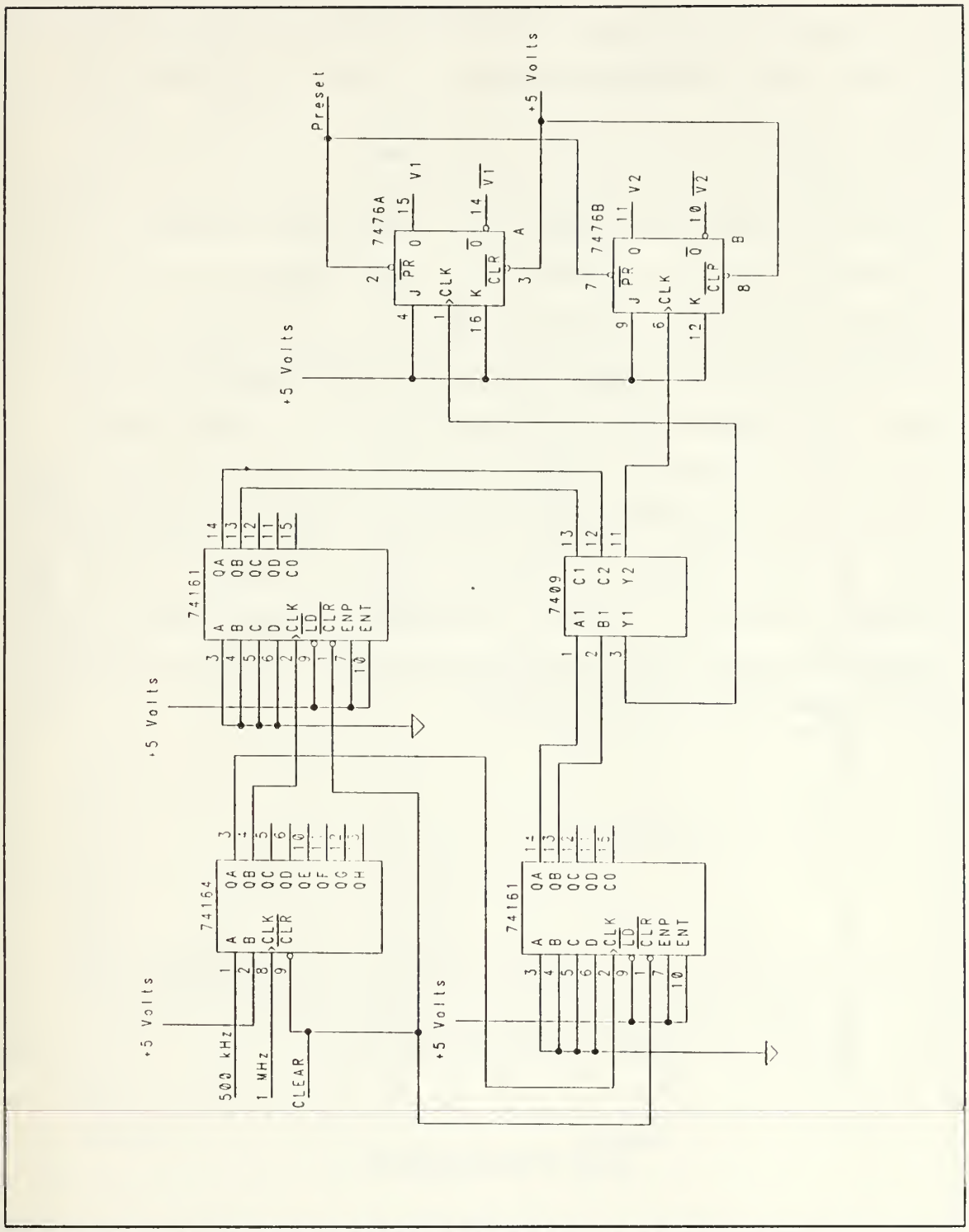

Figure 12. Implementation of Square Wave Ensemble Generator

of the filter began with the selection of two capacitors which were as closely matched in value as possible. The capacitance of individual capacitors varied between 960 and 1073 picoFarads. Pairs of capacitors were matched to within five picoFarads. The stock values of resistors R1 and R3 were chosen to have values as indicated in Table 3.2. The resistive value of R5 was then varied in order to adjust the filter center frequency to 62.5 kHz. The filter output consisted of a sinusoid with the same phase relative to the input square wave but shifted by 180 degrees due to the inverting configuration of the filter. Experimentation yielded a needed value of R5 between 15 kohms and 20 kohms in order to achieve the appropriate input/output relationship. The exact required value of the resistance, R5, was implemented by placing a five kohm adjustable pot in series with either a 13 or 16 kohm fixed resistor, as each filter required a different component value for R5. Figures 14 and 15 display the measured phase and magnitude characteristics of a typical filter implementation. The amplitude of the output set of sinusoids varied by up to twenty percent amongst members of the set. This amplitude variation was removed by the second filter stage. The second stage provided an ancillary benefit of inverting the input waveform and returning the output ensemble to an in phase relationship with the input. In addition to the 180 degree inversion, a three to six degree phase shift was noted across the second stage of the filter. This shift was compensated for by adjusting R5 in the first circuit stage.

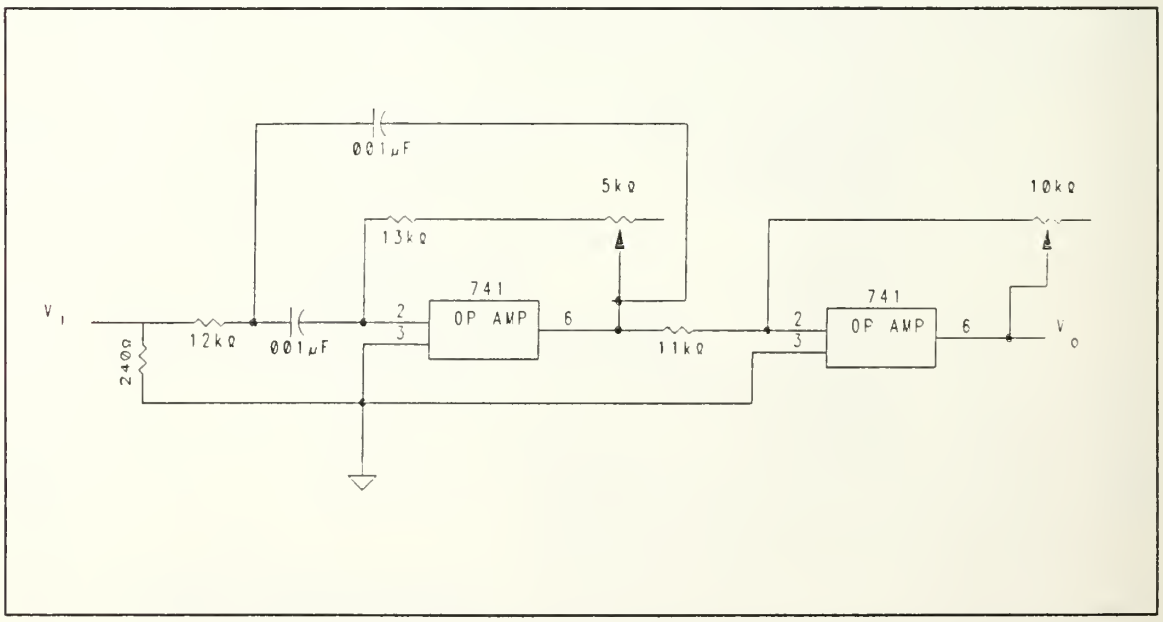

Figure 13. Implementation of Two Stage Active Filter

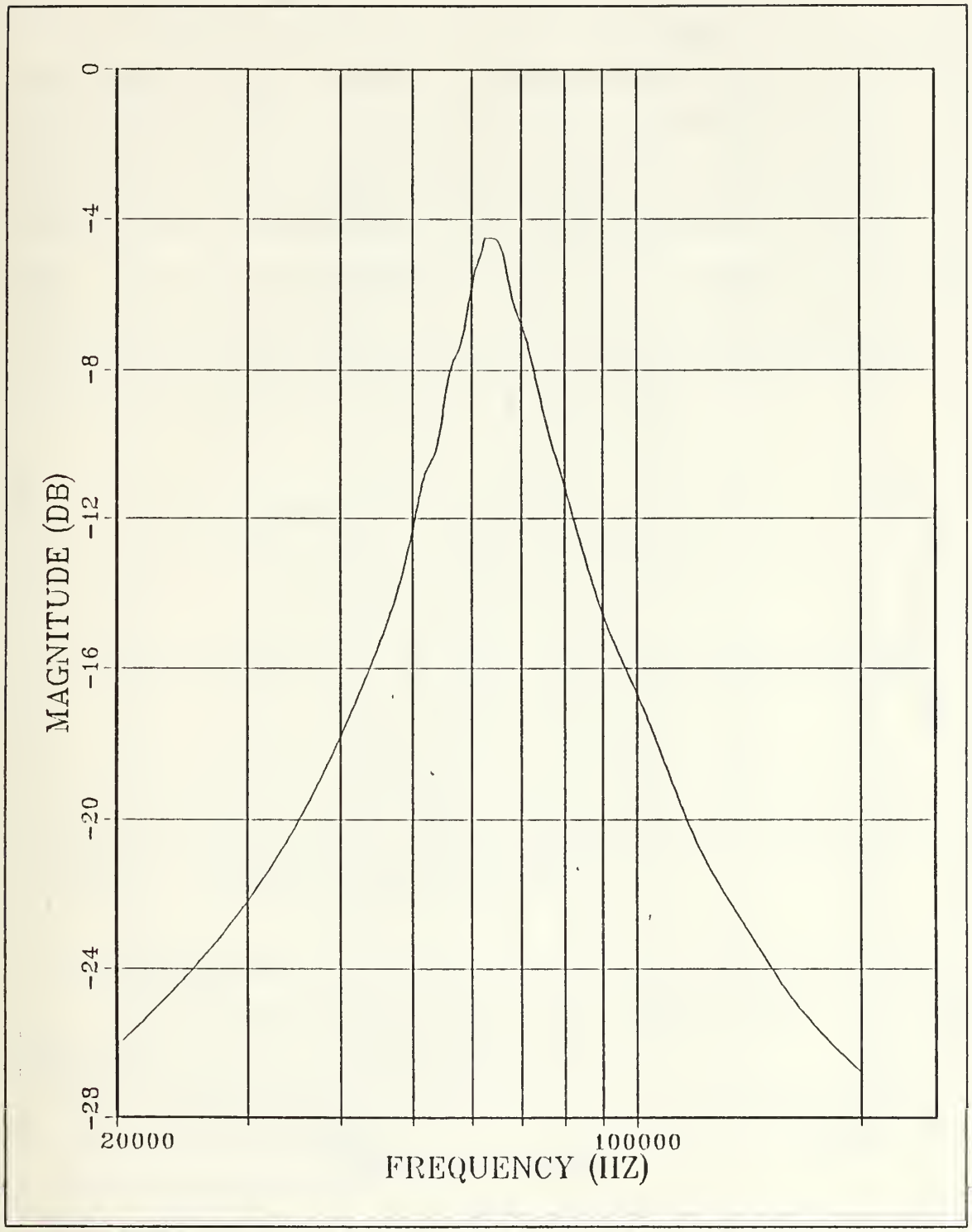

Figure 14. Single Stage Bandpass Filter Magnitude Response

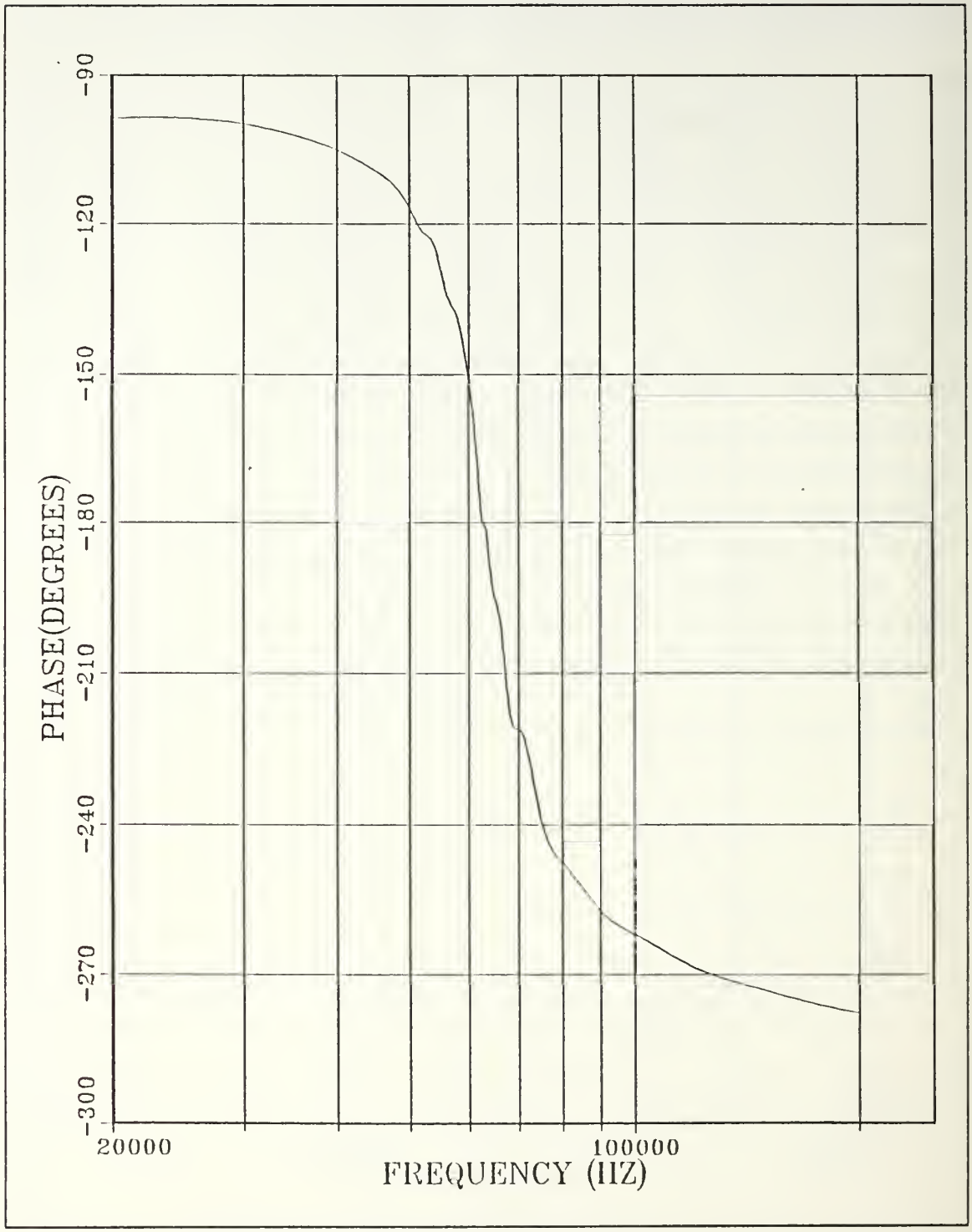

Figure 15. Single Stage Bandpass Filter Phase Response

c. Basis Functions

The sine and cosine basis functions were obtained via the same process which generated the signals described in the previous section except that a third filter stage, as shown in Figure 16, was added to the filter of Figure 13. The process of regenerating the basis functions was initiated by extracting a second output from stages eight and four of the shift register shown in Figure 4. Square waveforms $\overline{V8}$ and V4 were then regenerated and filtered to produce a second set of cosine and sine signals respectively. These signals were then applied to the input of the phase shifter. The phase shift across this final stage of the filter was controlled by adjusting the 10 kohm variable resistor shown in Figure 16. These two signals were each phase rotated by + 11.25 degrees to produce the functions necessary for coherent demodulation.

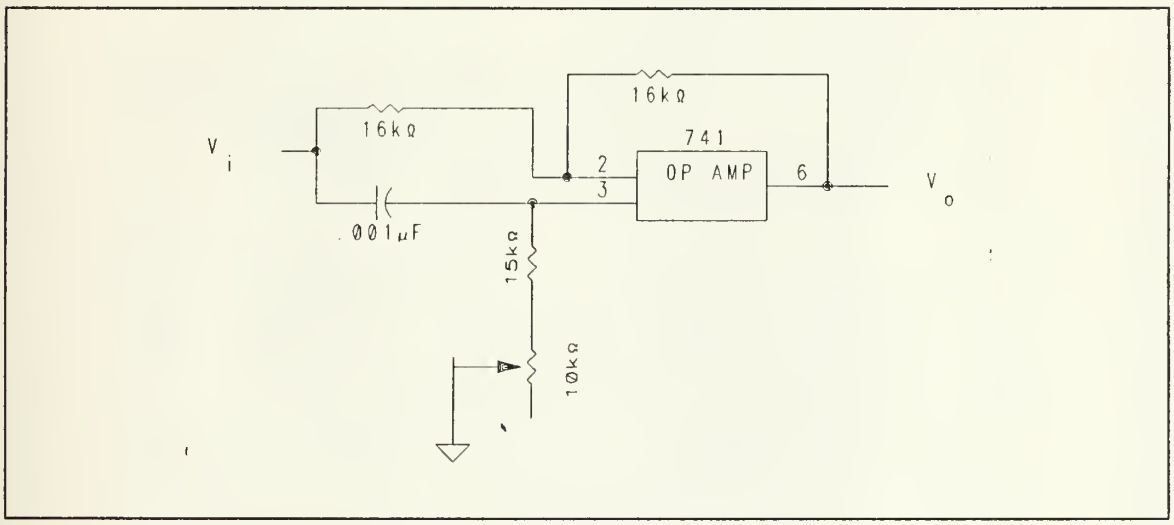

Figure 16. Implementation of Phase Shifter

2. Data Sequence

The data generator implementation is shown in Figure 17 [Ref. 1: p. 68]. The implementation consists of the following components:

74164 8 Stage Shift Register

7486 Quad Dual Input XOR

7400 Quad Dual Input NAND

7430 8 Input NAND

The circuit clock is a pulse signal provided by a WAVETEK signal generator. The M-sequence is generated as described in the section III.A.2. In order to ensure that an all

zero state does not arise in the FSR, an all zero detector/reset circuit is included in the data generator implementation [Ref. 1: p. 68]. The protection is provided by applying the output of each shift register stage to the input of the eight input NAND gate. This output is then paired with the inverted output of the third XOR gate and processed by a two input NAND gate. The output of the NAND gate is again inverted and fed to the first stage of the shift register. If the all zero state is encountered, the circuit will input a *logical* 1 to the first stage of the register and the M-sequence will restart. The detector will not affect the other FSR state combinations of the system.

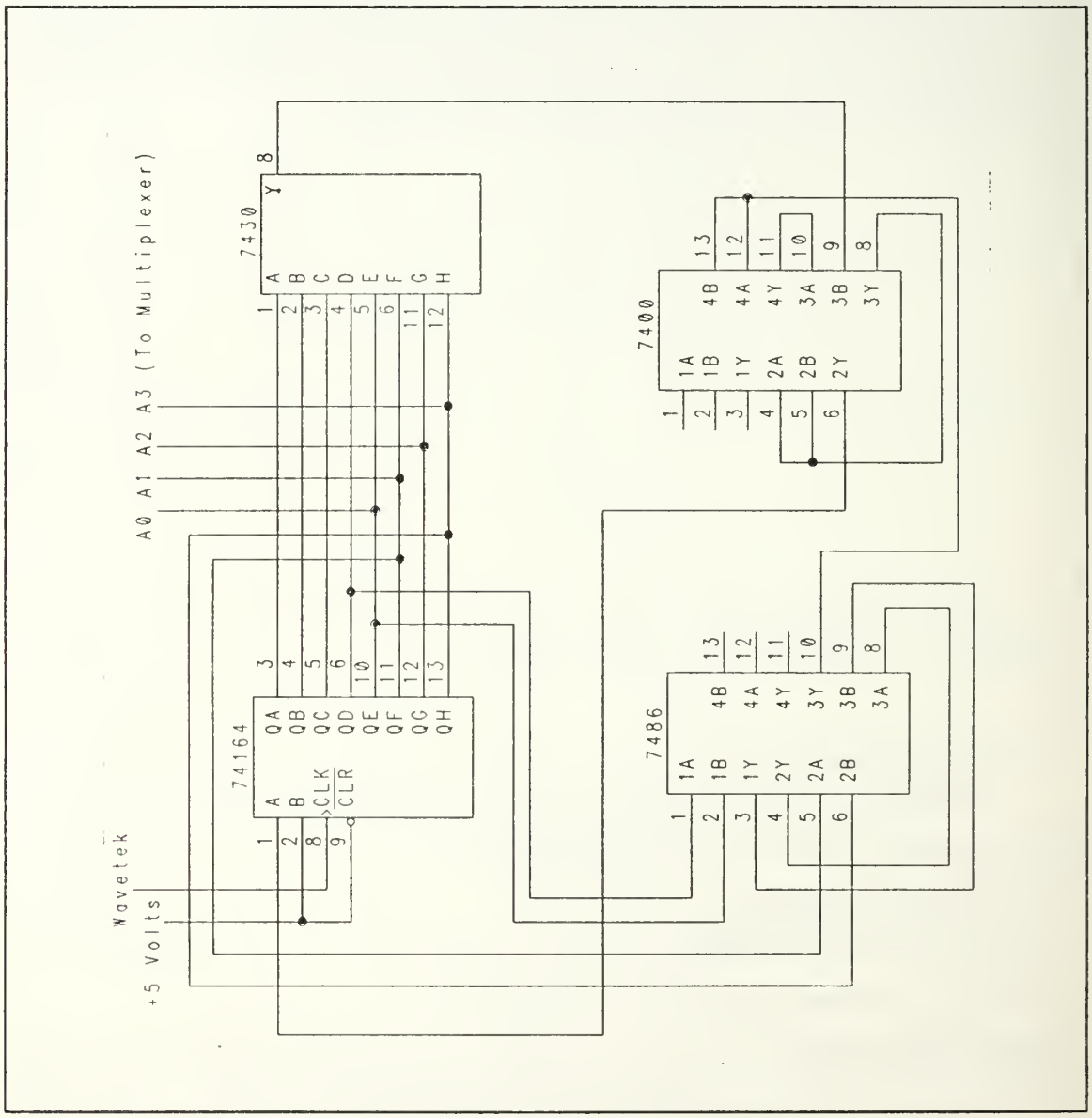

Figure 17. Implementation of Data Generator

3. Multiplexer

The device chosen for the multiplexer implementation is a DG506A 16-Channel Analog Multiplexer. This device is essentially a digitally controlled switch. The symbol represented by the four data bits A0 through A3 is provided by stages six through eight of the FSR respectively. Upon receiving a symbol input a switch closes within the multiplexer and the selected sinusoidal waveform from the ensemble of 16 phase shifted carriers is transferred to the output of the chip. Figure 18 displays the multiplexer implementation.

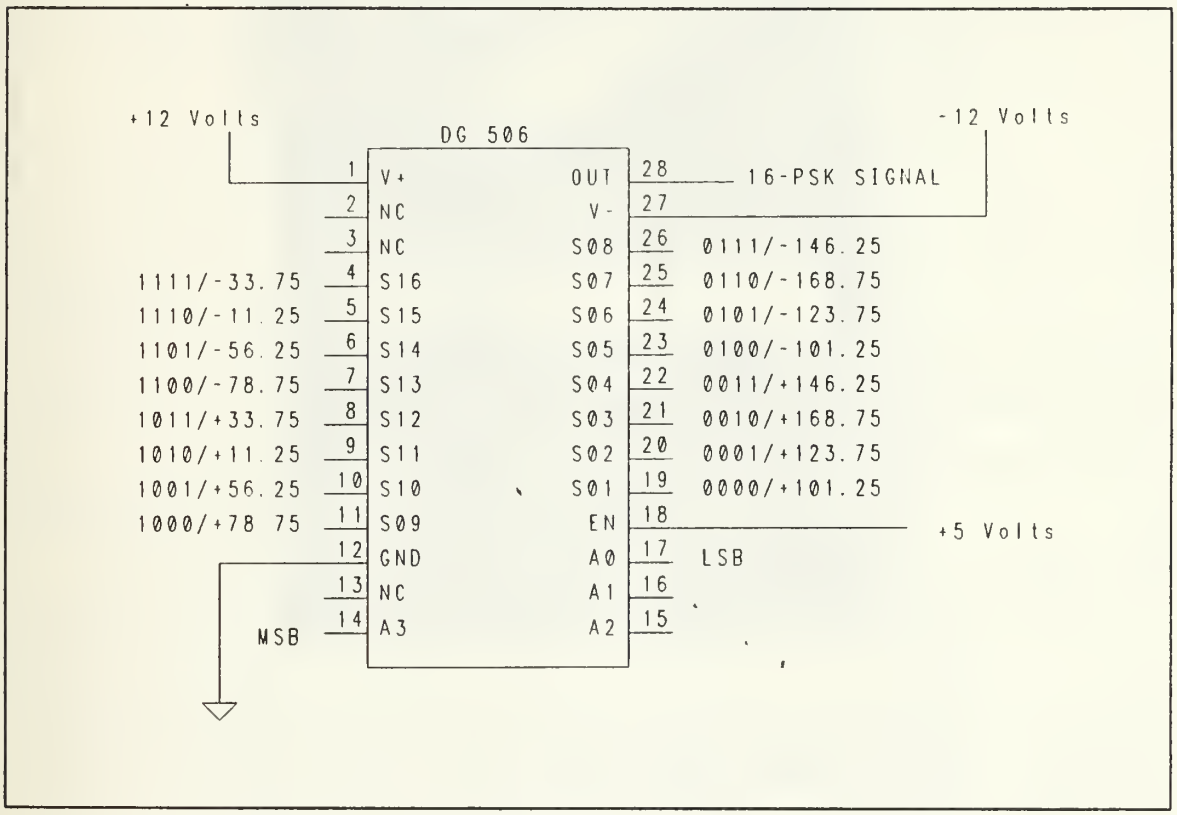

Figure 18. Implementation of Multiplexer

C. PHYSICAL IMPLEMENTATION

The physical implementation of the circuit described in the previous sections of this chapter is shown in Figure 19. Proceding from left to to right, the first *proto – board* contains the system clock, preset/clear pulse generator, and the circuit to generate the collection of square waveforms. The second *proto – board* contains the 18 single stage

bandpass filters which convert the set of square waves to a set of sinusoids. The third *proto – board* contains the second stage of each of the 18 filters and two analog phase shifters which provide the required phase rotation in order to produce the basis signals. The third *proto – board* also contains the multiplexer (largest chip), and the data sequence generator.

A photograph of the test bench layout is shown in Figure 20. The layout consists of the implemented circuit, its associated power supplies and the WAVETEK function generator which serves as a variable clock for the data sequence generator. The photograph also displays the gain/phase meter and oscilliscope which are utilized to record the system performance as highlighted in the next chapter.

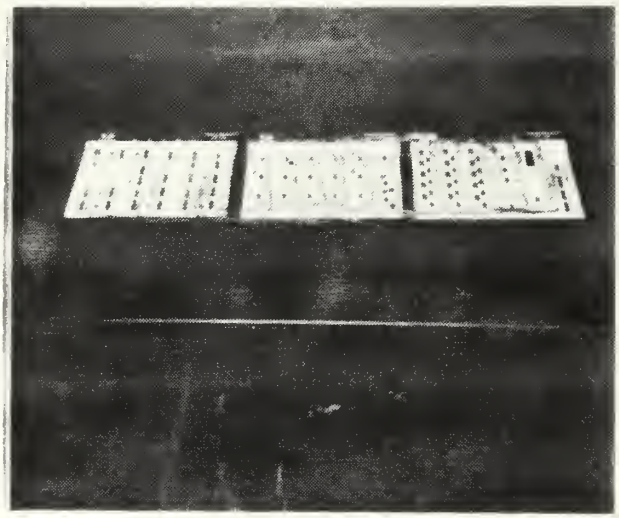

Figure 19. **Circuit Physical Implementation**

D. ALTERNATE IMPLEMENTATION

The implementation described in the previous section required the application of analog phase shifters in order to rotate the phase of the basis functions. This application could have been avoided if the implementation had been designed to generate square waves with appropriate relative delays such that extraction of thier fundamental component would produce sinusoids separated in phase by 11.25 degrees instead of 22.5 degrees. The square waves from which the basis functions are derived could then be produced directly by the shift register. This would eliminate the need for the application

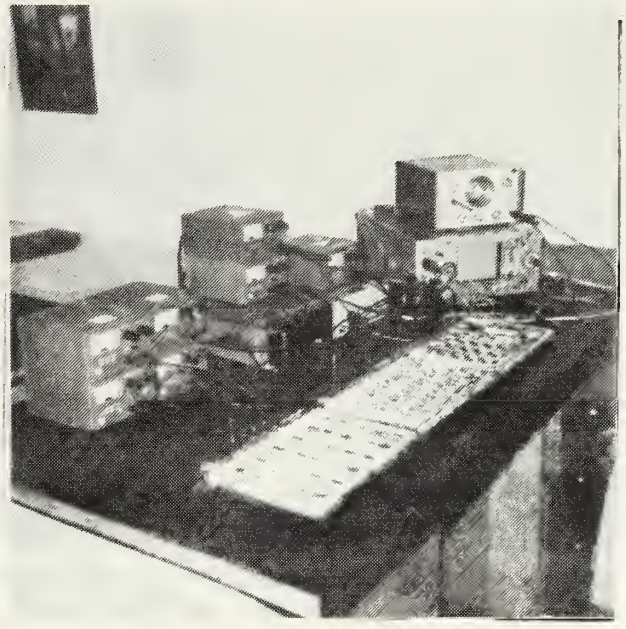

Figure 20. Test Bench Layout.

of the phase shifter. In this alternate implementation, an ensemble of 32 equally delayed square waves ($2^n = 32$, and $n = 5$) could be produced by utilizing a 16 stage shift register ($2^{(n-1)} = 16$). This alternative would take full advantage of digital techniques in order to generate exact phase shifts.

The filtering process employed in this implementation could also be obtained with a variety of alternative configurations. The implementation described in Reference 2 utilized a two stage Generalized Impedance Converter (GIC) filter design in order to implement a similarly constrained bandpass filter whose application dealt with generating a 2FSK/QPSK signal constellation. The GIC configuration has a low sensitivity to variations in passive component values. The lower sensitivity would increase the accuracy with which individual filters could be matched. Although the sensitivity of the GIC produces an overall superior implementation, it does not possess the flexibility to easily control the amplitude and phase of the filter output. The filter implemented and described in section III.B.1.b. does yield significant flexibility for controlling amplitude and phase characteristics.

IV. SYSTEM PERFORMANCE

This chapter describes the performance of the system described in Chapter III in terms of accuracy and stability. Photographs of time domain signals are presented to demonstrate the 16-PSK signal constellation and basis function generation. Measured frequency characteristics are presented to display the spectra of the random data sequence and multiplexer output. Results shown in this chapter were obtained with the HP3575A Phase Gain meter in order to provide amplitude and phase measurements, and the HP8566C Spectrum Analyzer in order to record frequency domain performance.

A. 16-PSK SIGNALS

Figures 21 through 24 are photographs of oscilloscope displays which show members of the signal ensemble (constellation shown in Figure 1). Each photograph presents the relationship in time between the unshifted cosine signal, which is the sinusoid that was generated by passing waveform $\overline{V8}$ shown in Figure 4 through the two stage filter shown in Figure 13, and specified signals within the constellation. In each figure, the horizontal axis measures time scaled at five microseconds per division, and the vertical axis measures amplitude scaled in 0.4 volts per division. The implementation achieved the desired phase relationships to within one tenth of a degree while the signal gain ratios were maintained to within one tenth of a decibel which represents the measurement accuracy of the HP3575A.

The system stability was measured by turning the system on and allowing it to warm up for an hour, then aligning and recording the initial phase and gain relationships. The unshifted cosine signal was chosen as a reference for the measurements. After five and one half hours of operation, the phase and gain relationships were again measured. The average phase drift of a signal with respect to its original phase alignment was found to be +0.273 degrees. The phase drift varied from signal to signal with a maximum of one half of a degree and a minimum phase drift of one tenth of a degree. No variation in gain ratios was observed. A second observation was recorded after 18.5 hours of operation. The signals continued to drift in phase, but the rate of drift decreased substantially. The average drift between signals when compared to the previous reading was observed to be +0.160 degrees. The phase drift varied between a maximum of three tenths of a degree and a minimum of zero degrees. Again, no variation in gain ratios was observed.

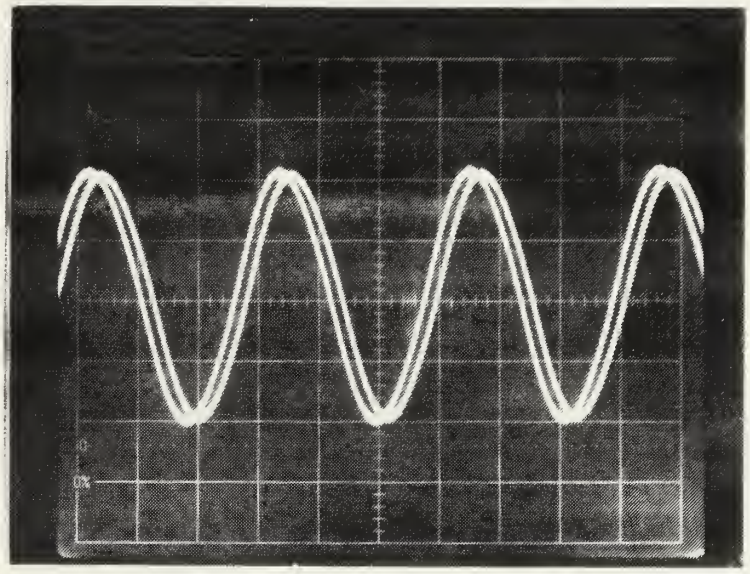

Figure 21. Unshifted Cosine and -22.5 Degree Phase Shifted Signal

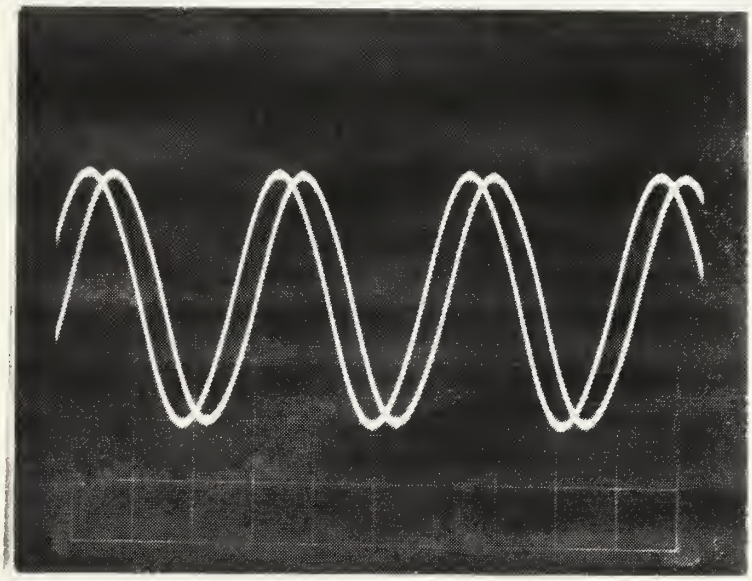

Figure 22. Unshifted Cosine and -45.0 Degree Phase Shifted Signal

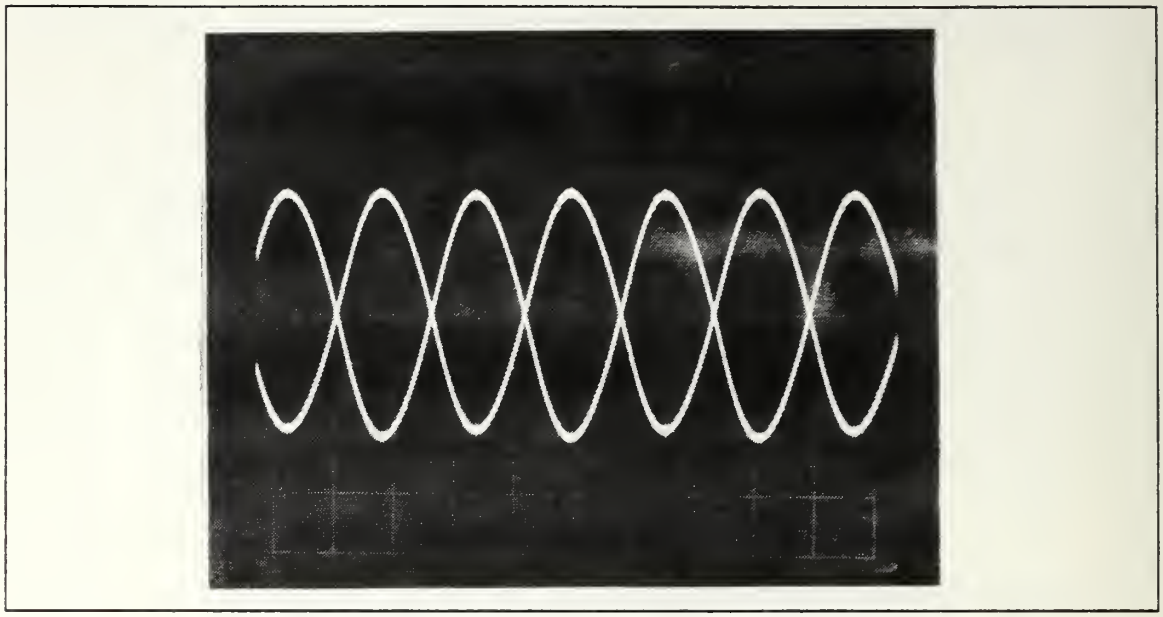

Figure 23. Unshifted Cosine and -90.0 Degree Phase Shifted Signal

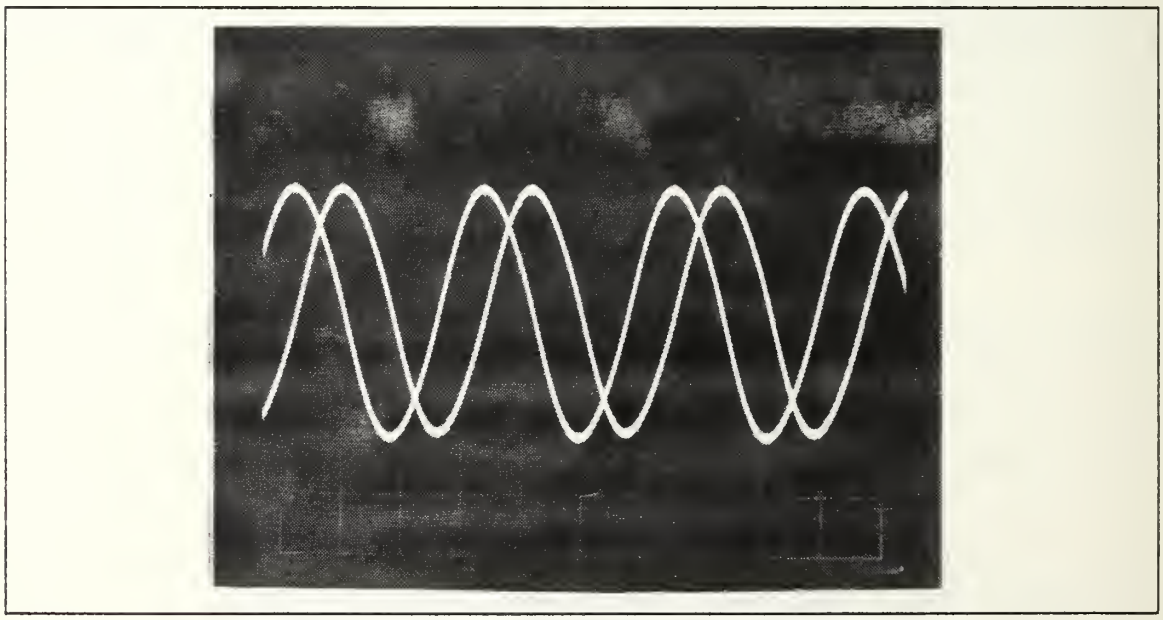

Figure 24. Unshifted Cosine and 180.0 Degree Phase Shifted Signal

B. BASIS FUNCTIONS

Figure 25 displays the unshifted cosine signal of Figure 1 and the basis function signal which was generated by reproducing the unshifted cosine signal and then applying

it to the input of the phase shifter of Figure 16. The output of the phase shifter is a sinusoid whose phase is shifted by +11.25 degrees with respect to the signal applied at its input. The calibration of the display axes is the same as noted in the previous photographs. The sine signal was also regenerated and rotated in this manner to produce the second basis function. The accuracy with which the phase rotation could be carried out was limited by the measurement accuracy of the HP3575A. The signals could be rotated by either +11.2 or +11.3 degrees by adjusting the phase shifter. The gain ratio could be concurrently matched to within one tenth of a decibel.

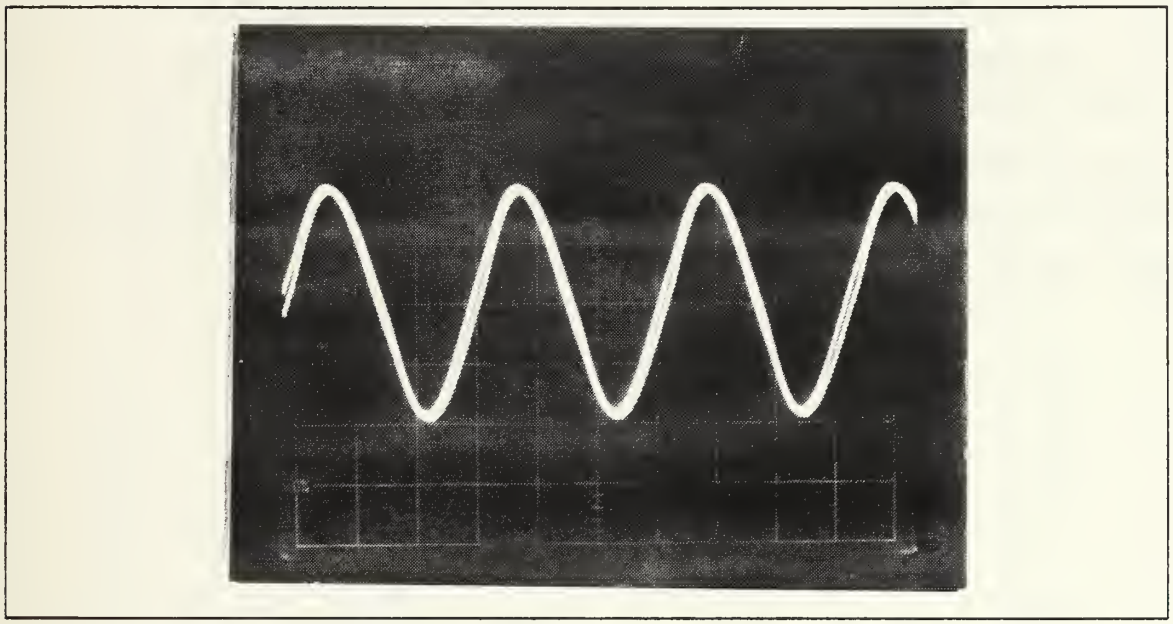

Figure 25. Original Cosine and Cosine Phase Shifted by +11.3 degrees

The stability of the basis functions was tested by the method outlined in the preceding section. The phase stability of the basis functions was comparable to that of the previously tested signals. Both basis signals drifted by one tenth of a degree over the initial five and one half hour test period. An additional one tenth of a degree phase drift was observed after 18.5 hours of operation. The gain ratio of these two signals did not vary throughout the stability test.

C. DATA SEQUENCE

The behavior of the data sequence was measured by observing the Power Spectral Density (PSD) of the M-sequence produced by the FSR. The theoretical PSD of this psuedorandom data stream is a $\frac{\sin x}{x}$ squared type function as shown in Figure 9 but

down-converted to baseband frequencies. Figure 26 shows the one sided PSD of the FSR output as measured by the HP8566C Spectrum Analyzer. The center frequency of the display is 5.1 kHz. The figure displays frequencies which range between a minimum value of 100 Hz and a maximum value of 10.1 kHz. Nulls occur at integer multiples of the bit rate frequency, which was set at two kilohertz for this measurement.

D. MULTIPLEXER

The output of the Multiplexer is a 16-PSK signal whose PSD is depicted in Figure 9, with nulls occurring at the symbol rate frequency. The symbol rate for this measurement is the same as the bit rate of the M-sequence produced by the FSR. This relationship results because the symbol is composed of the four bits taken from the last four stages of the FSR. Each time the FSR is clocked, the symbol changes and one bit exits from the last stage of the FSR. Figures 27 and 28 show the PSD of the multiplexer output for clock rates of 2KHz and 4KHz respectively.

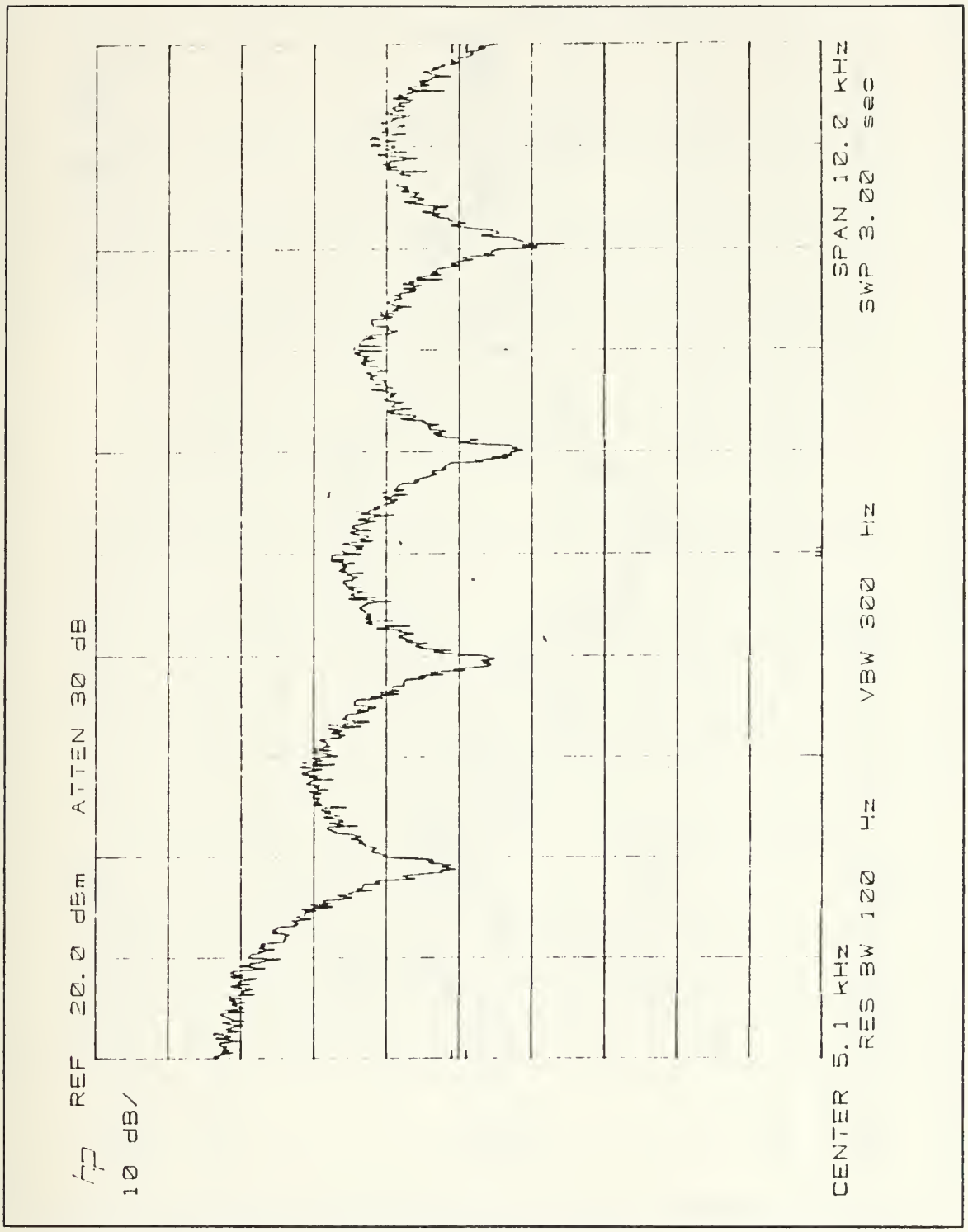

Figure 26. M-Sequence Power Spectral Density

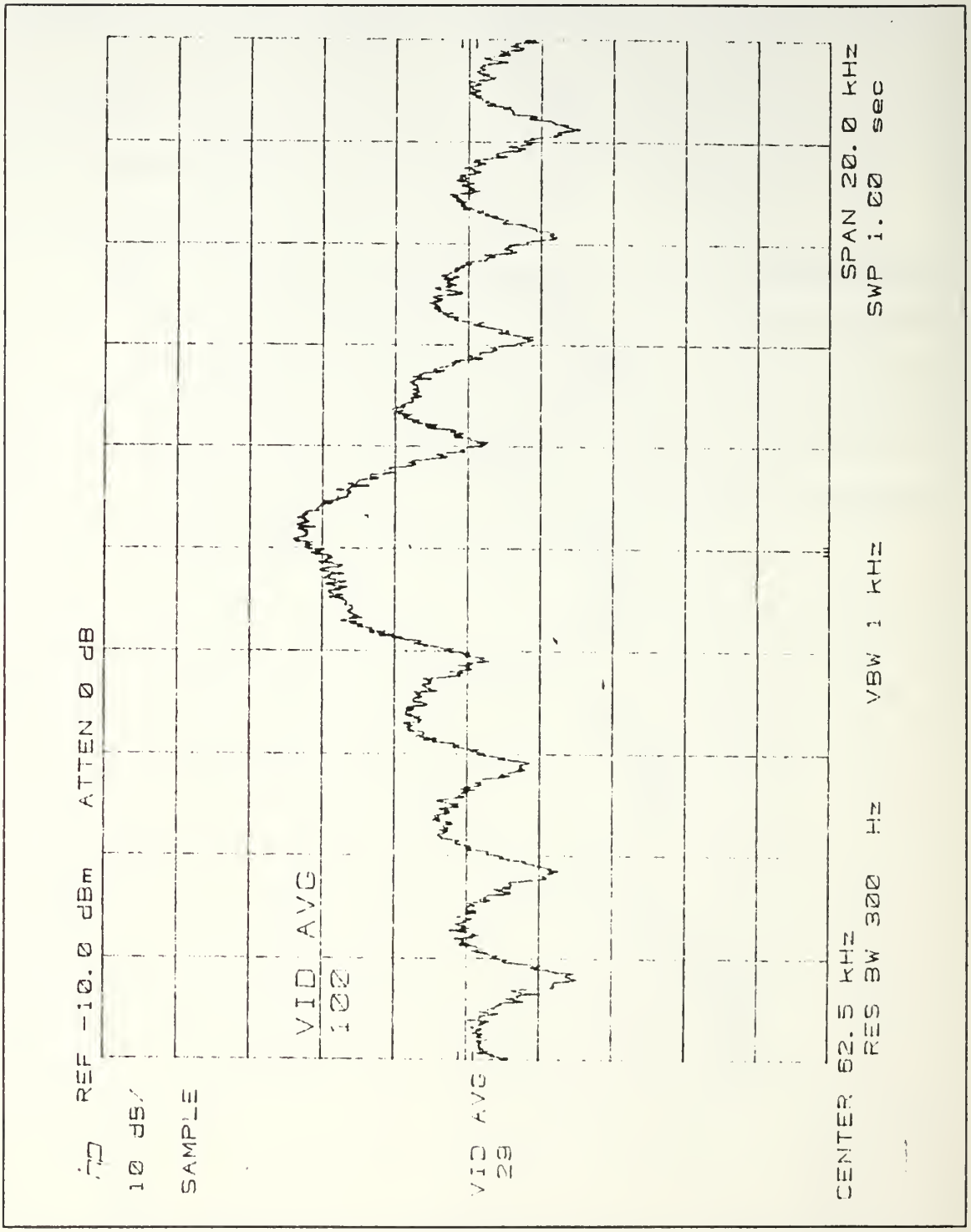

Figure 27. Power Spectral Density of 16-PSK Signal (Symbol Rate = 2 kHz)

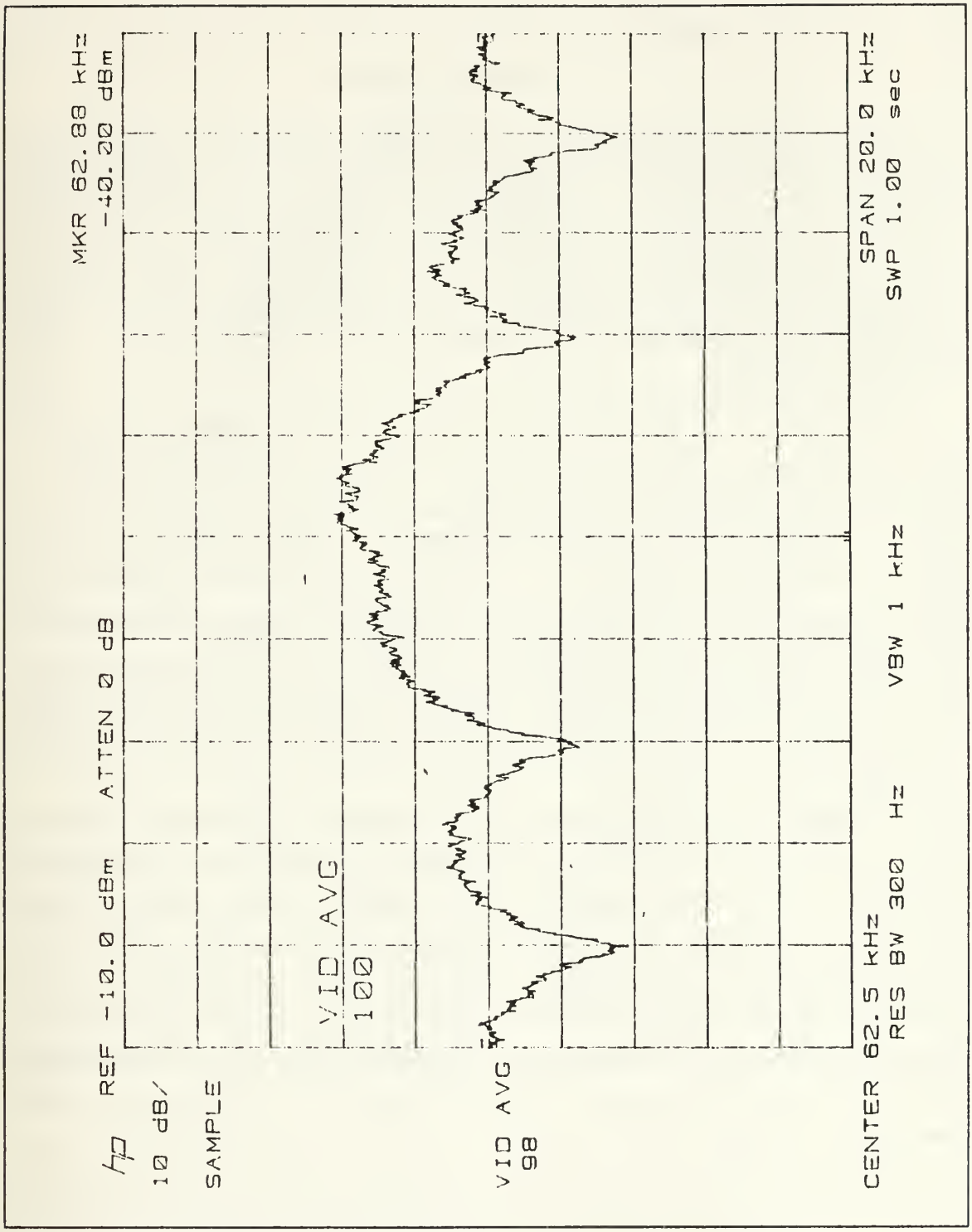

Figure 28. Power Spectral Density of 16-PSK Signal (Symbol Rate = 4 kHz)

V. CONCLUSIONS

This thesis effort was undertaken in order to demonstrate the feasibility of implementing an accurate and stable transmitter for generating 16-PSK modulated signals, ultimately, such a transmitter is intended for use in conjunction with a specific (not as yet implemented) direct bit detection (DBD) receiver. The design, implementation, and testing of the transmitter involved addressing four separate subtopics, namely the signal constellation and its generation, basis functions, the data sequence generation, and the multiplexer operation.

The bulk of the work described in this thesis involves the generation of the 16-PSK signal constellation. The method utilized to produce the desired signal constellation is based upon the design outlined in Reference 3 which can be directly attributed to the accuracy and stability realized by the implementation. The generation of the basis functions was done as an adjunct to the main effort in order to facilitate follow-on testing of the (not as yet implemented) coherent (DBD) receiver. The implementation of the data sequence generator and multiplexer are straightforward extensions of previous designs as described in References 1 and 2. The process utilized to generate this transmitter provides the accuracy and stability required for generation of higher order M-PSK modulated signals, i.e., $M > 16$.

As the order of an M-PSK signal constellation increases, each signal becomes more sensitive to the accuracy with which the phase of adjacent signals may be generated and maintained. The act of shifting the phase of a sinusoidal carrier is achieved through delaying a signal in time. The generation of a collection of waveforms which possess accurate and stable time relationships is a problem which is best solved by digital techniques. The design outlined in Reference 3 is based on the concept that highly accurate and stable systems for generating M-PSK modulated signals may be implemented by basing the transmitter design upon a digital foundation. The digital circuitry which provides this foundation is able to produce exact time delays and frequency divisions. A self clocking shift register is employed in a manner analagous to a tapped delay line in order to create an incremental time delay between successive stage outputs. The direct relationship that exists between this time delay and the phase shifts among members of a chosen M-PSK signal constellation specifies the frequency of the square wave input to the shift register once an operating frequency is specified. The process of digital

frequency division transfers the high frequency set of waveforms present at the shift register stage outputs to a collection of waveforms at the operating frequency which possess the desired time relationships.

Extensions of this specific design for M = 16 to higher order applications (M > 16) is most sensitive to the process of frequency selective filtering. The direct transfer of the time and amplitude relationships of the collection of square waves to a collection of sinusoids with appropriate phase relationships requires the implementation of M identical bandpass filters. Adjustments in the 16 filters of this implementation in order to achieve these relationships would become impractical for higher order constellations. Higher order implementations will require filtering schemes which possess lower sensitivity to variations in component values, or components with more restrictive tolerance on their characteristics.

The generation of basis functions as described in this thesis is an implementational requirement imposed to facilitate the follow on testing of a specific receiver structure. The method employed to generate these basis functions produced signals whose accuracy and stability was comparable to that of the other members of the signal constellation. The method of regeneration and analog phase rotation utilized is more easily implemented than the alternative of implementing digital circuitry designed to produce signals for a higher order constellation as discussed in Chapter III.D. For the case under consideration here, this would imply generating 32-PSK modulated signals.

The design is oriented toward the generation of signal constellations whose member's phase relationships are equally spaced and unchanging, while extension to the generation of signals possessing unequal or varying phase relationships cannot be efficiently implemented with this methodology. An inherent restriction of the design is the relationship between the operating frequency and the higher frequency input to the shift register. The operating frequency of this implementation was selected because of its compatibility with the available system clock. Working backwards from the operating frequency may generate a requirement for a system clock which is not readily available.

APPENDIX RECEIVER OPERATION AND PERFORMANCE

A. OPERATION OF THE DIRECT BIT DETECTION (DBD) RECEIVER

PSK signals are demodulated by coherent receivers. The block diagram of Figure 29 [Ref. 6: p. 462], shows a representation of the process which a conventional M-PSK symbol detection receiver employs in order to recover the transmitted symbol. The signals $s_0(t)$ through s_{M-1} (t) are replicas of the signals which comprise the transmitter signal constellation. The received signal, which is assumed to consist of only the transmitted signal plus noise, is correlated with each member of the set of signals $s_0(t)$ through $s_{M-1}(t)$. The correlation process produces a DC value at the output of each correlator which will be largest for that correlator in which the transmitted signal and the correlator signal $s_i(t)$ match, provided no noise is present. Noise will clearly affect this DC value which in practice will result in receiver decision errors. In practice, M-PSK receivers are implemented by recovering the in-phase (cosine) and quadrature (sine) components of the carrier. Each of these components is defined as a basis function. The received signal is then correlated with these components on two separate channels. Each correlator yields a DC value proportional to the dot product of the vector representing the basis function and the vector representing the received signal over a symbol duration. These two DC values are then processed to recover the transmitted symbol, which in general consists of n bits. The receiver processes and combines these two DC voltages to yield a unique estimated signal phase value. This value is then compared with M possible stored values, and a symbol assignment is made based upon a closest match principle.

A Direct Bit Detection (DBD) receiver is designed to recover individual bits within the transmitted symbol by processing the outputs (i.e., quadrature components) of the above mentioned correlators. In order to support a DBD receiver scheme, the signal constellation of Figure 1 must be rotated to produce the type of constellation shown in Figure 2 for 16-PSK modulation. The assignment of a symbol to a specific signal (or vector) will depend upon the receiver design.

The symbol assignments shown in Figure 2 are based upon the receiver design shown in Figure 30 [Ref. 6: p. 462]. Tracing the path of the received signal (assuming for the moment no noise or other forms of interference are present) through the receiver reveals the logic behind the bit assignment scheme shown. As mentioned above, the correlation of the cosine (sine) basis function with the received signal will yield a DC

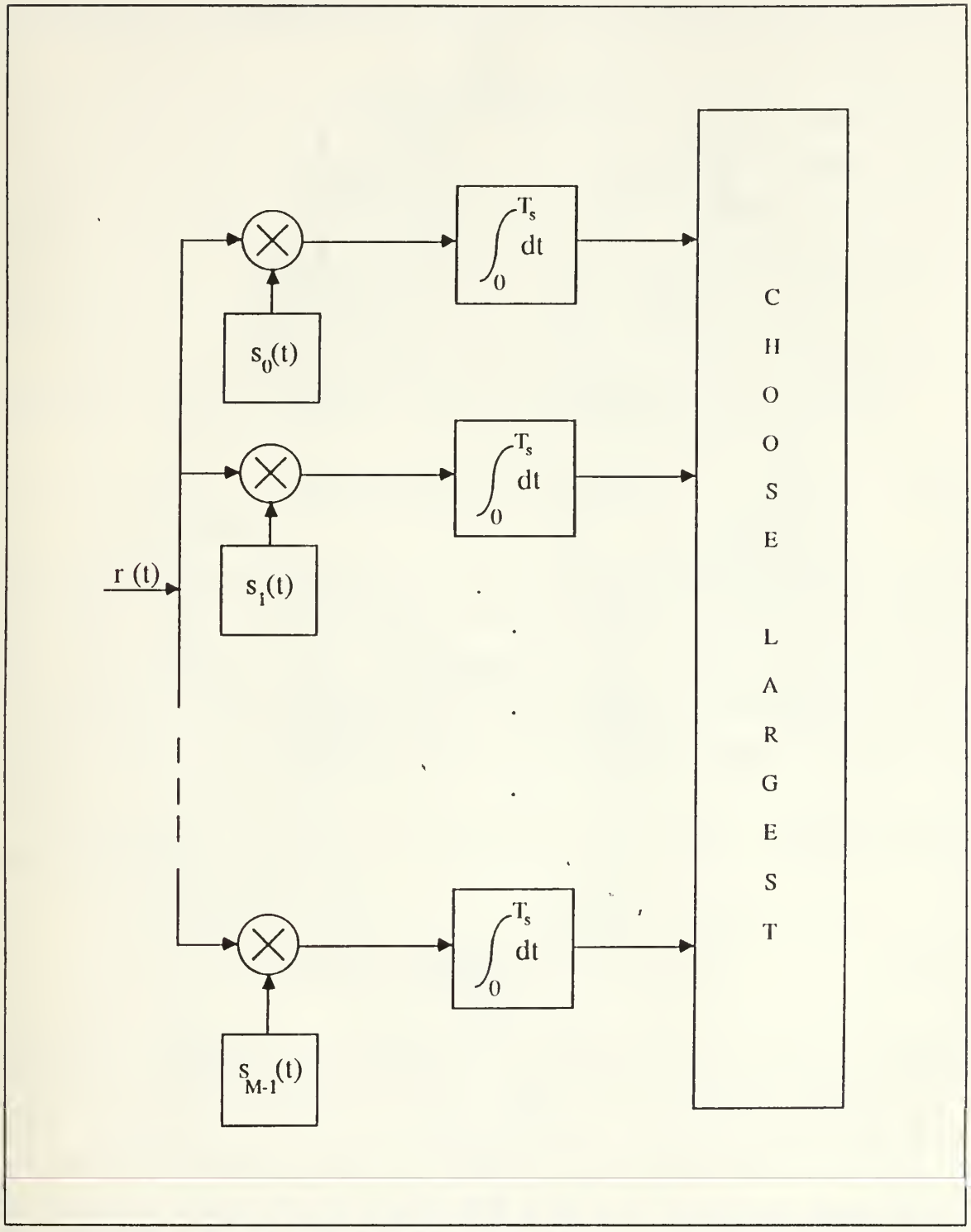

Figure 29. M-PSK Symbol Detection Receiver

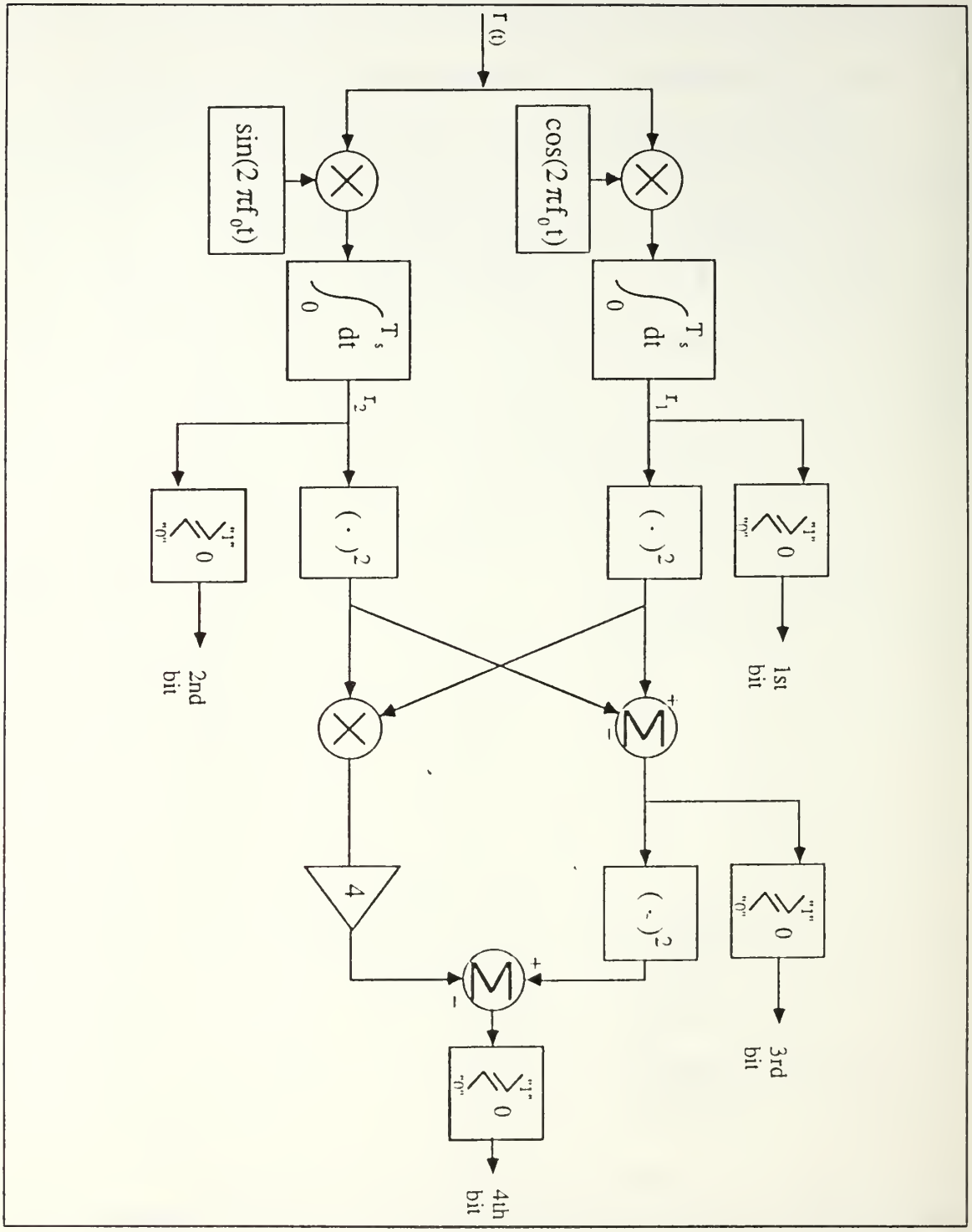

Figure 30. Direct Bit Detection (DBD) Receiver

value proportional to the projection of the vector representing the received signal upon the cosine (sine) axis. This projection will be positive for vectors lying in the right half plane of the constellation. The comparator assigns a first bit of *logical* 1 to right half plane vectors, and *logical* 0 to left half plane vectors. The second bit is determined by correlating the received signal with the sine basis function. This process similarly yields a second bit assignment of *logical* 1 for vectors lying the the upper half plane and *logical* 0 for those in the lower half plane because, as indicated above, the correlation of the sine basis function with the received signal will yield a DC value proportional to the projection of the vector representing the received signal upon the sine axis.

In Figure 30, the projection of the received vector on the cosine and sine axes is designated as r_1 and r_2, respectively. The process which determines the third bit is

$$(r_1)^2 - (r_2)^2 \begin{cases} > 0 = \textit{logical}\ 1 \\ < 0 = \textit{logical}\ 0 \end{cases} \qquad (A.1)$$

The result is a comparison between the cosine, and sine components which comprise each vector. The 45 degree line within each quadrant separates these two decision regions. The comparator assigns the eight vectors possessing a greater cosine projection than sine projection (in magnitude sense) a third bit of *logical* 1. The remaining vectors possess a larger sine than cosine component and are therefore assigned a third bit of *logical* 0.

The assignment of the fourth bit is more difficult to visualize. The process which determines the fourth bit is

$$((r_1)^2 - (r_2)^2)^2 - 4((r_1)^2(r_2)^2) \begin{cases} > 0 = \textit{logical}\ 0 \\ < 0 = \textit{logical}\ 1 \end{cases} \qquad (A.2)$$

The value of the first term is dependent upon the difference between r_1 and r_2. A large difference will yield a dominant first term, a positive sum, and a bit assignment of *logical* 0. Applying this observation to the constellation of Figure 2 reveals that within each quadrant, the difference term $r_1^2 - r_2^2$ will be largest for the two exterior vectors. The comparator assigns a fourth bit of *logical* 0 to the outer vectors and a fourth bit of *logical* 1 to the two interior vectors. An alternate visualization recognizes that this process is equivalent to multiplying the phase angle of the received signal by a factor of four and then computing the cosine of this new angle. This operation will yield positive

values for the outer vectors, and negative values for the interior vectors (further details of this important point may be found in Reference 6).

B. PERFORMANCE OF THE 16-PSK DBD RECEIVER

The performance of digital receivers is specified in terms of their Bit Error Rate (BER). The specific DBD receiver outlined in Figure 30 employs a unique process to recover each transmitted bit. Furthermore, the voltages which are processed to determine bit assignments are dependent upon the transmitted signal. For example if the symbol 1100 is transmitted, the voltage processed to determine the recovery of the first bit is proportional to the projection of the vector representing that signal upon the cosine axis (refer to Figure 2). This voltage would be considerably less than the voltage available for processing if the symbol 1110 were to be transmitted. The consequences of this recovery scheme are that the error rate will vary, depending upon which signal is transmitted, and which of the four bits that constitute a symbol is being evaluated. The theoretical bit error rates for this specific receiver were derived in Reference 6 and are displayed below.

$$P_r(1\text{st bit}_{incorrect}) = \frac{1}{4}\left[Q\left(\sqrt{\frac{2E_s}{N_0}}\cos 11.25^\circ\right) + Q\left(\sqrt{\frac{2E_s}{N_0}}\cos 33.75^\circ\right)\right] + \frac{1}{4}\left[Q\left(\sqrt{\frac{2E_s}{N_0}}\sin 33.75^\circ\right) + Q\left(\sqrt{\frac{2E_s}{N_0}}\sin 11.25^\circ\right)\right] \quad (A.3)$$

with

$$P_r(1\text{st bit}_{incorrect}) = P_r(2\text{nd bit}_{incorrect}) \quad (A.4)$$

$P_r(\text{3rd bit}_{incorrect}) =$

$$\frac{1}{2}Q\left(\sqrt{\frac{E_s}{N_0}}(\cos 11.25° - \sin 11.25°)\right) + Q\left(\sqrt{\frac{E_s}{N_0}}(\cos 11.25° + \sin 11.25°)\right)$$

$$x\left[\frac{1}{2} - Q\left(\sqrt{\frac{E_s}{N_0}}(\cos 11.25° - \sin 11.25°)\right)\right] \qquad (A.5)$$

$$+ \frac{1}{2}Q\left(\sqrt{\frac{E_s}{N_0}}(\cos 33.75° - \sin 33.75°)\right) + Q\left(\sqrt{\frac{E_s}{N_0}}(\cos 33.75° + \sin 33.75°)\right)$$

$$x\left[\frac{1}{2} - Q\left(\sqrt{\frac{E_s}{N_0}}(\cos 33.75 - \sin 33.75°)\right)\right]$$

$$
\begin{aligned}
&P_r(4\text{th bit}_{incorrect}) = \\
&\frac{1}{2} - \sqrt{\frac{E_s}{\pi N_0}} \int_0^{\frac{\pi}{8}} e^{-\left(\frac{E_s}{N_0}\right)\sin^2(\Gamma - 11.25^\circ)} \cos(\Gamma - 11.25^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \cos(\Gamma - 11.25^\circ) \right) \right\} + e^{-\left(\frac{E_s}{N_0}\right)\cos^2(\Gamma - 11.25^\circ)} \sin(\Gamma - 11.25^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \sin(\Gamma - 11.25^\circ) \right) \right\} + e^{-\left(\frac{E_s}{N_0}\right)\cos^2(\Gamma + 11.25^\circ)} \sin(\Gamma + 11.25^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \sin(\Gamma + 11.25^\circ) \right) \right\} + e^{-\left(\frac{E_s}{N_0}\right)\sin^2(\Gamma + 11.25^\circ)} \cos(\Gamma + 11.25^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \cos(\Gamma + 11.25^\circ) \right) \right\} \qquad (A.6) \\
&+ e^{-\left(\frac{E_s}{N_0}\right)\sin^2(\Gamma - 33.75^\circ)} \cos(\Gamma - 33.75^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \cos(\Gamma - 33.75^\circ) \right) \right\} + e^{-\left(\frac{E_s}{N_0}\right)\cos^2(\Gamma - 33.75^\circ)} \sin(\Gamma - 33.75^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \sin(\Gamma - 33.75^\circ) \right) \right\} + e^{-\left(\frac{E_s}{N_0}\right)\cos^2(\Gamma + 33.75^\circ)} \sin(\Gamma + 33.75^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \sin(\Gamma + 33.75^\circ) \right) \right\} + e^{-\left(\frac{E_s}{N_0}\right)\sin^2(\Gamma + 33.75^\circ)} \cos(\Gamma + 33.75^\circ) \\
&\times \left\{ \frac{1}{2} - Q\left(\sqrt{\frac{2E_s}{N_0}} \cos(\Gamma + 33.75^\circ) \right) \right\} d\Gamma
\end{aligned}
$$

In the above equations, E_s represents the energy per symbol, which is four times the energy per bit, E_b. The overall PEB may be computed by weighting the error probabilities of each bit by one fourth, and then summing the result. These results are graphically presented in Figure 31 [Ref. 6: p. 468]. The curves for the error rates of the first and second bits are identical due to the identity of Equation (A.4). For the third and fourth bits, the plots of Figure 31 show higher error rates than for the first and second bits, with the fourth bit exhibiting the highest error rate for given $\frac{E_b}{N_0}$ values. The overall

BER is also plotted in Figure 31, with corresponding values as a function of $\frac{E_b}{N_0}$ that has been shown (see Reference 6) to be optimum.

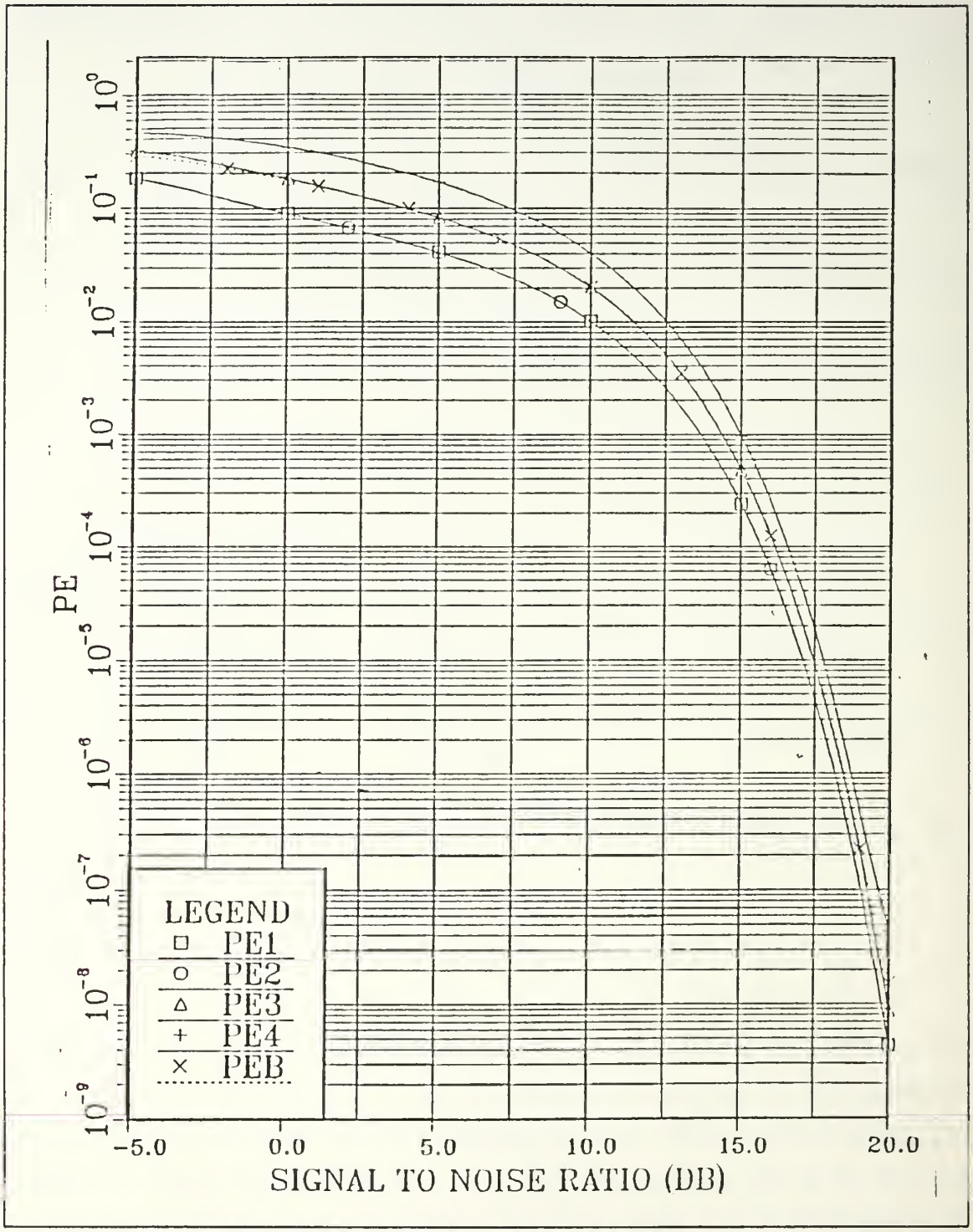

Figure 31. Theoretical Performance of 16-PSK DBD Receiver

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